Experimental Determination of the Toughness of Crack Stop Structures

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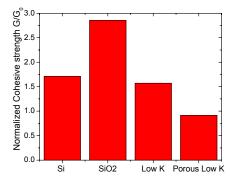
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Abstract

In this paper we present an experimental approach to the determining the toughness of crackstop structures. It is shown that methods used for adhesion testing can be adapted to quantitatively determine the effective toughness of different crackstop designs. A design based on metal pad shapes connected together with vias is shown to be capable of producing toughnesses that are 3.75 times the intrinsic toughness of the dielectric. In an optimized design we obtain a further 60% improvement in the crackstop toughness. The experiments presented provide an accurate way of determining the effectiveness of crackstop designs in arresting dicing flaws driven by the stresses present in different packages.

Introduction

A major challenge in packaging semiconductor die is to prevent cracks initiated at the edge of chips during dicing from propagating into the active area of a chip under the influence of thermal stresses that arise during packaging and use^{1,2}. In die that use SiO2 as a backend dielectric the toughness of the dielectric is higher to that of silicon and thus the silicon die its self often presents the weakest path by which cracks can propagate into the interior of the chip. With the introduction of CVD Low K dielectrics the fracture resistance of the dielectric has been substantially reduced and can be comparable or, as in the case of porous dielectrics, significantly lower that that of silicon (Figure 1). As a result, preventing cracking and delamination of the low K dielectric layers at the edge of a chip presents even more of a challenge under the stresses that arise from chip package interactions (CPI).



Figure(1) Relative cohesive strengths of BEOL dielectric materials.

One approach to preventing cracking at the edge of the chip is incorporate patterned metal structures around the perimeter that act as a crackstop by increasing the fracture resistance near the edge of the chip. In order to know how effective such structures are it is important to be able to measure the fracture resistance of such structures under realistic and controlled loading conditions. In this paper we present methods we have developed to access the fracture resistance of realistic crackstop structures and show that by using a four point bend loading geometry a quantitative measure of their fracture resistance, which can be used in predictive models of crackstop performance, can be obtained.

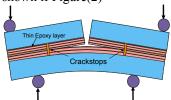
Experimental Results

Measurement of the effective toughening a crackstop design provides presents a similar problem to that of measuring the adhesion strength of interfaces and similar methods to those used in adhesion testing can be applied. In this paper we describe two different approaches to measuring the toughness of crackstops.

In the first the crackstop toughnesses is quantified using the Modified Edge Liftoff Test (MELT)^{3,4}. In this test cracks are driven in from the edge of the diced sample by a thick over coating of epoxy. The stress driving the cracks is provided by the thermal mismatch of the epoxy with the thin film substrate. As the temperature is lowered the driving force on edge delaminations increases and at a critical temperature they are driven in from the edge of the chip. This process closely mimics a common failure mode in CPI in wire bonded chips in which edge delaminations are propagated into the interior of a chip by the thermal stresses that arise from an overmold compound². For the crackstop evaluation an eight level chip with a porous Low K dielectric at four intermediate level was diced close to the crackstop structure after coating with a 130 um layer of MELT epoxy. The crack stop structure consisted of rows of fill shapes connected by vias which formed a continuous perimeter close to the edges of the diced chip. The structure was slowly cooled to liquid nitrogen temperatures on a cooling stage and the temperature at which cracks propagated in from the edge of the chip was noted. The crack driving force to cause failure of the crackstop can be estimated from thermo mechanical properties of the epoxy and the temperature at which failure occurs^{3,4}. For comparison a similar area chip without the crackstop was tested in the same manner. These structures failed in the low

K layers on dicing indicating a toughness that was comparable to that of the porous Low K dielectric G_0 . With the crackstop present the critical crack driving force energy increased to a value that was 3.4 times G_0 .

A more controlled and quantifiable test for adhesion is the four point bend test ^{5,6}. In this test a crack is driven in a thin film interface by gluing a dummy wafer onto a wafer with the thin film stack of interest deposited on it. The sandwich is cut into bend bars and a crack is initiated in the interface of interest from a saw notch cut in the middle of the bend bar. The crack is driven by loading the bar in a four point bend jig as shown if Figure(2)

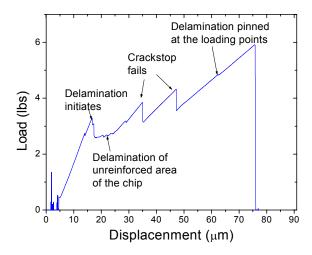


Figure(2) Four point bend test configuration for testing crackstop structures.

The advantage of this test is that at a given load the driving force on the crack is independent of crack length from short cracks up to where the crack approaches the loading points. Thus by measuring the load at which a crack advances the critical crack driving force can be calculated. We have applied the same test to chip structures that contain a crack stop. The structures used for the test were the same as those used for the MELT test experiments. The bend bars were cut from a sandwich that was made by gluing a dummy wafer onto the processed wafer. The notch in the bend bar was positioned mid way between two crack stop structures which were oriented across the width of the bar and lay 7.5 mm from the notch. To help initiate the crack a 3mm wide stripe of gold was deposited on the wafer at the position of the notch before that sandwich was glued together. This acted as a release layer and helped initiate the crack in the BEOL stack.

A typical load displacement trace for this sample is shown in Figure (3). The initial linear portion of the plot corresponds to elastic loading of the bar. The sharp drop in load is where the crack initiates and propagates into the release layer. In the plateau region that follows the crack is propagating in a region of the chip where there are no via structures to reinforce the chip. The load at the plateau is a measure of the toughness of the unreinforced region of the chip at the level that crack is propagating in. Once the cracks intersect the crackstops they arrest. The arrest of the crack at the crack stop was verified by monitoring the crack opening displacement in the region of the notch. Knowing the load and the geometry of the sample this opening can be calculated from simple beam theory for a given crack length. Hence the position of the crack can be carefully monitored by measuring the opening displacement. Further loading of the sample produces a linear increase load with

displacement which corresponds to elastic bending of the sample with little or no further crack extension. The peaks are the load needed for the crack to break through the crack stop and the peak load is a measure of the toughness of the crackstop. The second peak corresponds to fracture of the second crack stop on the second arm of the bend bar. The final linear portion of the trace is where the cracks have arrested at the loading points. From the peak loads at which the crackstops failed the critical crack driving force was found to be 2 to 2.5 times the cohesive strength of the dielectric (G₀). This fracture toughness corresponds to the effective toughness of a finite width crackstop.

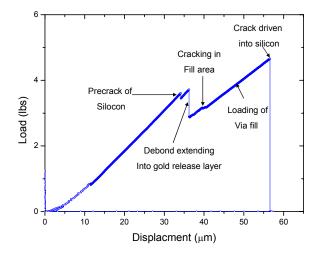


Figure(3) load displacement trace from four point bend testing of crackstops in an eight level BEOL structure.

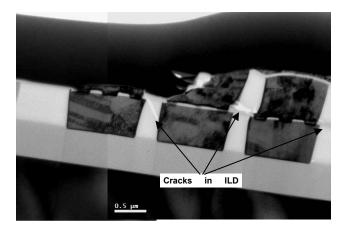
From models for fiber toughening the toughness of the via structures would be expected increase with crack stop width but eventually reach a plateau value that represents the maximum toughness attainable for a given design. To determine the maximum toughness achievable with the via structures a special purpose chip was designed which consisted of a two level metal structure with large areas of metal shapes connected by vias. A 0.4 cm strip of unreinforced structures (no vias) was included to act as a crack initiation region in 4 point bend testing. Bend bars for four point testing were prepared as described above. The crack initiation notch was located in the center of the unreinforced area of the chip. A load displacement trace from a typical test is shown in Figure(4)

The first peak corresponds to initiation of the crack. Only a short plateau is observed where the crack is propagating in the unreinforced area of the chip. The last linear region in the plot corresponds to loading when the crack is arrested by the crackstop. In each test, fracture of the bottom silicon bar coincided with failure of the crackstop. The location of the failure was confirmed by inspection the fracture surfaces in an optical microscope. It

was found that the crack extended five to six rows of fill shapes in from the edge of the reinforced area before being driven into the silicon below the crack stop or over the top of the crackstop structure. A TEM cross section of the edge of the failed region is shown in Figure(5).



Figure(4) load displacement trace from four point bend testing of a large array of via reinforced metal pads.



Figure(5) TEM cross section of the crack front produced by testing a via reinforced structure.

The picture shows cracks in the dielectric ahead of a region where the vias remain intact. Fracture through the vias can be seen on the right hand side of the image. This observation along with optical inspection of the crack front indicates that the cohesive zone created by the vias is fairly short (5-8 rows of vias). From the peak loads at which the crackstop failed the toughness of the infinite width crackstop was estimated to be $3.75~G_0$. This value is slightly larger than the fracture resistance obtained from the four point bend testing of a finite width crackstop and comparable to the value obtained from the MELT test. Theses observations show that even with a narrow crack stop toughnesses

approaching the maximum attainable with a given structure can be achieved. By further optimizing the crackstop design we have attained crackstop toughnesses of $6 G_0$.

In addition to static loading of the crackstop the crackstop can experience cyclic loading conditions during thermal cycling. Potentially this could lead to fatigue effects and premature failure of the crack stop at sub critical driving forces. To investigate the susceptibility of the crackstop to fatigue failure we loaded four point bend test specimens so as to extend the cracks up to the crack stop structures. The specimens were then repeatedly loaded to 80% of their critical failure load, each time cycling the load to zero before reloading. The crackstop remained intact after 3000 cycles indicating it was highly resistant to fatigue.

The toughness measurements presented in this paper provide a basis for evaluating the effectiveness of crackstops in arresting edge cracks in different packaging situations. The toughnesses obtained can be directly compared with the strain energy release rates obtained from packaging models. For comparison it is important that the experiments impose a similar mix of shear and tensile forces on the crack to those imposed by the package. The MELT test provides a loading that is dominated by tensile loading (Phase angle 25°) where as the 4 point bend test has almost equal shear and tensile contributions (Phase angle 45°). It is possible that this difference accounts for the slightly higher toughnesses obtained with the MELT test. From calculations we have made with a typical C4 type package it is found that the 4 point bend test better represents the kind of loading an edge crack produced by dicing would experience⁷. We have found that from a comparison of the crackstop toughnesses measured with the 4 point bend test with the calculated crack driving force obtained by finite element methods we can obtain an accurate assessment of the effectiveness of different crackstop configurations in accelerated tests such as deep thermal cycling.

References

- S. Sankaran et al. "A 45 nm CMOS node Cu/Low-k/Ultra Low-k PECVD SiCOH (k=2.4) BEOL Technology", IEDM Dec. 11-13, 2006.
- W. Landers et al.; <u>Proc. Of Int. Interconnect Tech. Conf.</u>, pp. 108-110, 2004.
- (3) Shaffer II, E. 0, Mills, M. E., Hawn, D., Van Ges-tel, M., Knorr, A., Gundlach, H., Kumar, K., Kaloyeros, A. E. and Geer, R. E., "Adhesion Energy Measurements of Multilayer Low-K Dielectric Mate-rials for ULSI Applications", Mat. Res. Sot. Symp.Proc. Vol. 511, pp. 133-138, 1998.
- (4) J. C. Hay, X-H Liu, and E. G. Liniger "Numerical Mechanics of delamination in multifilms on substrates" J. Mater. Res 16(2), 385 (2001).
- (5) Cao HC, Evans AG. "An experimental study of the fracture resistance of bimaterial interface". Mech Mater 1989;7:295– 305.
- (6) Z. Huang, Z. Suo,*, G. Xu, Jun He, J.H. Prevost, "Initiation and arrest of an interfacial crack in a four-point bend test", Engineering Fracture Mechanics 72 (2005) 2584–2601
- (7) X. H. Liu, T. M. Shaw., M. W. Lane, E. G. Liniger, B. Herbst, D. Questad Chip-Package-Interaction Modeling of Ultra Lowk/Copper Back End of Line IITC 2007.