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Micro-Raman spectroscopy and analysis of near-surface stresses in silicon around through-silicon vias for three-dimensional interconnects

Suk-Kyu Ryu,[1] Qiu Zhao,[2] Michael Hecker,[3] Ho-Young Son,[4] Kwang-Yoo Byun,[4] Jay Im,[2] Paul S. Ho,[2] and Rui Huang[1,a)]
[1]*Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, Texas 78712, USA*
[2]*Microelectronics Research Center, University of Texas, Austin, Texas 78712, USA*
[3]*GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, 01109, Dresden, Germany*
[4]*Hynix Semiconductor Inc., Icheon-City, Gyeonggi-do, Korea*

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Three-dimensional integration with through-silicon vias (TSVs) has emerged as an effective solution to overcome the wiring limit imposed on device density and performance. However, thermal stresses induced in TSV structures raise serious thermomechanical reliability concerns. In this paper, we analyze the near-surface stress distribution in a TSV structure based on a semi-analytic approach and finite element method, in comparison with micro-Raman measurements. In particular, the depth dependence of the stress distribution and the effect of elastic anisotropy of Si are illustrated to properly interpret the Raman data. The effects of the surface oxide layer and metal plasticity of the via material on the stress and Raman measurements are discussed. The near-surface stress characteristics revealed by the modeling and Raman measurements are important for design of TSV structures and device integration. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3696980]

I. INTRODUCTION

Three-dimensional (3D) integration has emerged as an effective approach to overcome the wiring limit imposed on chip performance, density and power consumption beyond the current technology.[1–4] Through-silicon vias (TSVs) are important elements for 3D integration providing direct die-to-die connections to form stacked structures. However, there are mechanical stresses due to the introduction of these elements, which may become critical for function and reliability of the chips. For example, the thermal expansion mismatch between a typical copper (Cu) TSV and silicon (Si) can induce thermal stresses sufficiently high to cause failure of the integrated TSV structures due to cracking or interfacial delamination.[5–10] Moreover, the stresses around TSVs may degrade the performance of nearby electronic devices through the piezoresistivity effect.[11,12] It is thus essential to measure and analyze the stress characteristics in the TSV structures. Among several potential techniques, the micro-Raman spectroscopy appears particularly promising and was recently applied to measure the local stress distribution in Si near Cu TSVs.[13–15] This method is a spectroscopic technique where the stress magnitude is deduced from the frequency shift of the impinging laser light as a result of inelastic scattering by Si lattice.[16–18] The lateral resolution of micro-Raman spectroscopy is in the order of 0.5 μm, depending on the laser wavelength and the substrate lattice.[18] For Si, the Raman penetration depth ranges up to $\sim$2 μm, again depending on the laser wavelength. Moreover, this technique can be used to measure the near-surface stresses in Si around TSVs even with an oxide layer covering the wafer surface because the laser can penetrate the oxide layer with nearly 95% transparency.

In this paper, we present micro-Raman measurements along with numerical analyses of the near-surface stress distribution in a TSV structure. Section II briefly reviews the theory of Raman spectroscopy for stress measurement. Section III describes the TSV specimen and the results of micro-Raman measurements. A detailed stress analysis is presented in Sec. IV, based on a semi-analytical approach for an isolated TSV and the finite element method for a periodic array of TSVs. In Sec. V, the numerical results are compared to the Raman measurements, and the effects of the surface oxide layer and metal plasticity in the Cu vias are discussed.

II. THEORY OF RAMAN SPECTROSCOPY

The effect of strain (ε_{ij}) on the Raman modes in (001) silicon is described by the secular equation[19]

$$\begin{vmatrix} p\varepsilon_{11}+q(\varepsilon_{22}+\varepsilon_{33}) & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22}+q(\varepsilon_{33}+\varepsilon_{11}) & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33}+q(\varepsilon_{11}+\varepsilon_{22}) \end{vmatrix} - \lambda \mathrm{I} = 0, \tag{1}$$

where p, q, and r are material parameters representing the phonon deformation potential. For a unstrained silicon, there are three degenerated Raman modes with the same frequency ($\omega_0 \sim 520.8\,\mathrm{cm}^{-1}$) but different polarizations:[20] two transverse optical modes (TO) and one longitudinal optical (LO) mode. With strain, the three optical modes in general have different frequencies (ω_i) and different intensities (I_i), corresponding to three Raman peaks. The eigenvalues of the secular equation predict the Raman frequency shifts, $\Delta\omega_i = \omega_i - \omega_0 \approx \lambda_i/(2\omega_0)$. The intensity of the Raman

a)Electronic mail: ruihuang@mail.utexas.edu.

signal for each optical mode depends on the polarization vectors of the incident and scattered light. Most Raman systems have a backscattering configuration, where the incident light is nearly perpendicular to the sample surface. For backscattering from (001) silicon, only one of the three Raman modes is observable.

For the TSV specimen as illustrated in Fig. 1(a), the near-surface stress in Si is approximately biaxial, represented as $(\sigma_r, \sigma_\theta)$ in a cylindrical coordinate for the radial and circumferential stresses.[10] For Raman scanning along the [110] direction, the frequency shift for the observable Raman mode is related to the stress components as

$$\Delta\omega_3 = \frac{\lambda_3}{2\omega_0} = \frac{pS_{12} + q(S_{11} + S_{12})}{2\omega_0}(\sigma_r + \sigma_\theta), \qquad (2)$$

where S_{11} and S_{12} are components of the elastic compliance tensor. Thus, the sum of the two stress components can be measured from the Raman shift. To determine the effective proportionality factor between the Raman shift and the stress sum for the specific experimental conditions, calibration measurements by high-resolution X-ray diffraction (XRD) on an equibiaxially stressed film system were conducted, yielding the relation[13]

$$\sigma_r + \sigma_\theta \text{ (MPa)} = -470\Delta\omega_3(\text{cm}^{-1}). \qquad (3)$$

The obtained sensitivity factor corresponds to phonon deformation potential parameters in between of the theoretical values derived by Chandrasekhar *et al.*[21] and Anastassakis *et al.*[22] Note that the reference frequency ω_0 also depends on the system calibration, typically with $\pm 0.02\,\text{cm}^{-1}$ spectral resolution, which corresponds to a stress resolution of ~10 MPa.[23,24] In the present study, this quantity was determined at positions far away from the TSVs assuming that the stress there was below the minimum detection level.

III. EXPERIMENT

The TSV specimen used in the present study consists of a periodic array of Cu vias of diameter $D = 10\mu$m in a (001) Si wafer, with the pitch distances of 40 μm in [110] direction and 50 μm in the perpendicular direction. The TSV structure near the wafer surface is schematically shown in Fig. 1(a). An oxide layer of about 0.4 μm thickness and a thin Ta barrier layer were deposited on the sidewall between the via and Si. The surface of the Si wafer was covered by an oxide layer of about 0.8 μm thickness; for some measurements the surface oxide layer was mechanically polished off. The wafer thickness was 700 μm, and the via depth was around 55 μm.

A Jobin Yvon spectrometer HR800 was used for the Raman measurements, equipped with 442 nm Ar excitation laser and a focused spot size of about 0.8 μm by a 100× objective (NA = 0.9). The lateral resolution of the Raman measurements also depends on the laser scanning step, which was between 0.1 and 0.5 μm in the present study. The penetration depth (d) of the laser radiation is approximately 200 nm into Si in this case. Figure 1(b) shows the measured Raman intensity and frequency around two neighboring vias obtained by a line scan along the [110] direction, and Fig. 1(c) shows a representative Raman spectrum. The effects of laser power on the full-width at half-maximum (FWHM) and the signal-to-noise ratio were measured in order to determine the optimum laser power for the Raman measurements. In particular, the laser power was reduced by filters to a level that heating of the Si (in principle visible as line shift and broadening) was below the detection limit. The suitable laser power density was found to be around 2 mW/μm^2. In Fig. 1(b), the drop in the intensity of the Raman signal indicates the locations of the Si/TSV interface. Close to the interface, the Raman frequency first drops and then rises abruptly.

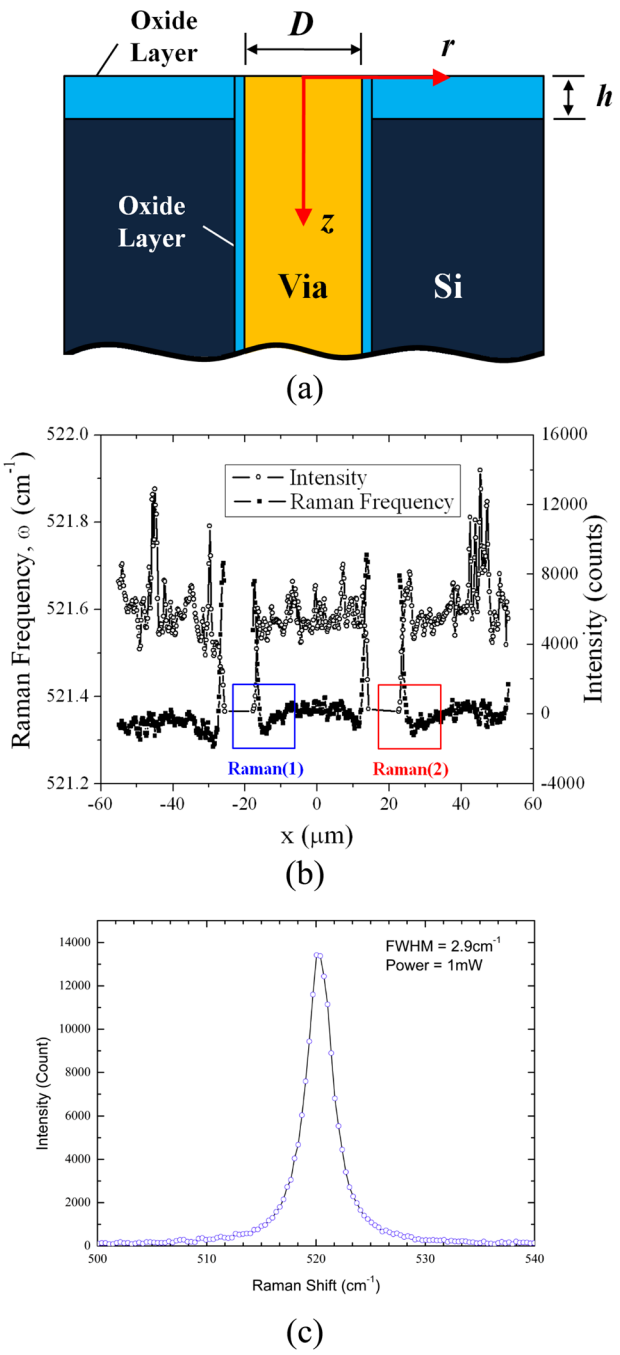

FIG. 1. (a) Schematic of a fully filled TSV structure near the wafer surface; (b) measured Raman intensity (unfilled symbols) and frequency (filled symbols) around two Cu vias in a periodic array; (c) a representative Raman spectrum.

With Eq. (3) and a calibrated reference frequency ω_0, the sum of the two principal stresses in Si can be deduced directly from the Raman frequency shift, which presumably is a volume average over the region defined by the area of the focused spot and the penetration depth of the laser. As shown in a previous study, the near-surface stress field induced by differential thermal expansion around a TSV is nonuniform in both in-plane and depth directions.[10] Therefore, it is important to interpret the micro-Raman measurement along with a detailed stress analysis.

IV. ANALYSIS OF NEAR-SURFACE STRESSES

The stresses in the TSV structures may result from both thermal and athermal contributions.[25] However, the athermal contribution is typically process dependent, which is unknown for the TSV specimen as received in the present study. To account for the athermal effect, we take an empirical approach by assuming a reference temperature at which the specimen is stress free. The choice of the reference temperature was based on curvature measurements of bending beam specimens with similar TSV materials and structures reported in a previous study.[26] The near-surface stresses of the TSV specimen are then calculated by taking the thermal load (ΔT) from the reference temperature to the room temperature ($\sim 30\,^{\circ}\mathrm{C}$).

First, as a semi-analytical approach, the stress field induced by differential thermal expansion around a circular via embedded in a Si wafer can be obtained approximately by the method of superposition. The result consists of a 2D plane-strain solution to the classical Lame problem subjected to a thermal load (ΔT) and a 3D near surface solution due to a surface pressure.[27] Together, the stress components are obtained in an integral form:[10]

$$\sigma_r(r,z) = \frac{-E\varepsilon_T}{2(1-\nu)}\left(\frac{D}{2r}\right)^2 - \frac{E\varepsilon_T}{2\pi(1-\nu)}\int_0^{\frac{D}{2}}\int_0^{2\pi} \left[\left(\frac{1-2\nu}{R^2+Rz} - \frac{3z(R^2-z^2)}{R^5}\right)\cos^2\beta + \left(\frac{z}{R^3} - \frac{1}{R^2+Rz}\right)(1-2\nu)\sin^2\beta\right]\rho\, d\rho\, d\theta, \quad (4)$$

$$\sigma_\theta(r,z) = \frac{E\varepsilon_T}{2(1-\nu)}\left(\frac{D}{2r}\right)^2 - \frac{E\varepsilon_T}{2\pi(1-\nu)}\int_0^{\frac{D}{2}}\int_0^{2\pi} \left[\left(\frac{1-2\nu}{R^2+zR} - \frac{3z(R^2-z^2)}{R^5}\right)\sin^2\beta + \left(\frac{z}{R^3} - \frac{1}{R^2+zR}\right)(1-2\nu)\cos^2\beta\right]\rho d\rho d\theta, \quad (5)$$

$$\sigma_z(r,z) = \frac{E\varepsilon_T}{1-\nu}\left[-1 + \int_0^{2\pi}\int_0^{\frac{D}{2}} \frac{3z^3\rho d\rho d\theta}{2\pi R^5}\right], \quad (6)$$

$$\sigma_{rz}(r,z) = \frac{E\varepsilon_T}{1-\nu}\int_0^{2\pi}\int_0^{\frac{D}{2}} \frac{3z^2(r-\rho\cos\theta)\rho\, d\rho\, d\theta}{2\pi R^5}, \quad (7)$$

where $R = \sqrt{z^2+r^2+\rho^2-2\rho r\cos\theta}$, $\beta = \tan^{-1}((\rho\sin\theta)/(r-\rho\cos\theta))$, and $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$ is the thermal mismatch strain. A cylindrical coordinate is used with $z = 0$ at the wafer surface and $r = 0$ at the via center [see Fig. 1(a)].

Here we have assumed that the via material has the same elastic modulus as Si and have ignored other materials such as the oxide layers. The material parameters, α, E, ν, are the coefficient of thermal expansion (CTE), Young's modulus, and Poisson's ratio, with the subscripts f and m for the via (fiber) and Si (matrix), respectively. For quantitative calculations, the following material parameters were used: $E_f = E_m = E = 130\,\mathrm{GPa}$, $\nu_f = \nu_m = \nu = 0.28$, and the CTE mismatch, $\Delta\alpha = \alpha_f - \alpha_m = 14.7\,\mathrm{ppm}/^{\circ}\mathrm{C}$. Furthermore, a thermal process of cooling from a reference temperature down to the room temperature with $\Delta T = -100\,^{\circ}C$ is assumed. Figure 2(a) shows the near-surface stress components at $z = 0.2\ \mu$m. Clearly, the radial and circumferential stresses in Si are dominant, while the other stress components are negligibly small except for the locations very close to the TSV/Si interface. Thus, the stress state in Si is nearly biaxial at this depth. Moreover, the radial and circumferential stresses are in opposite signs, with relatively high magnitudes near the TSV/Si interface and approaching zero far away from the via.

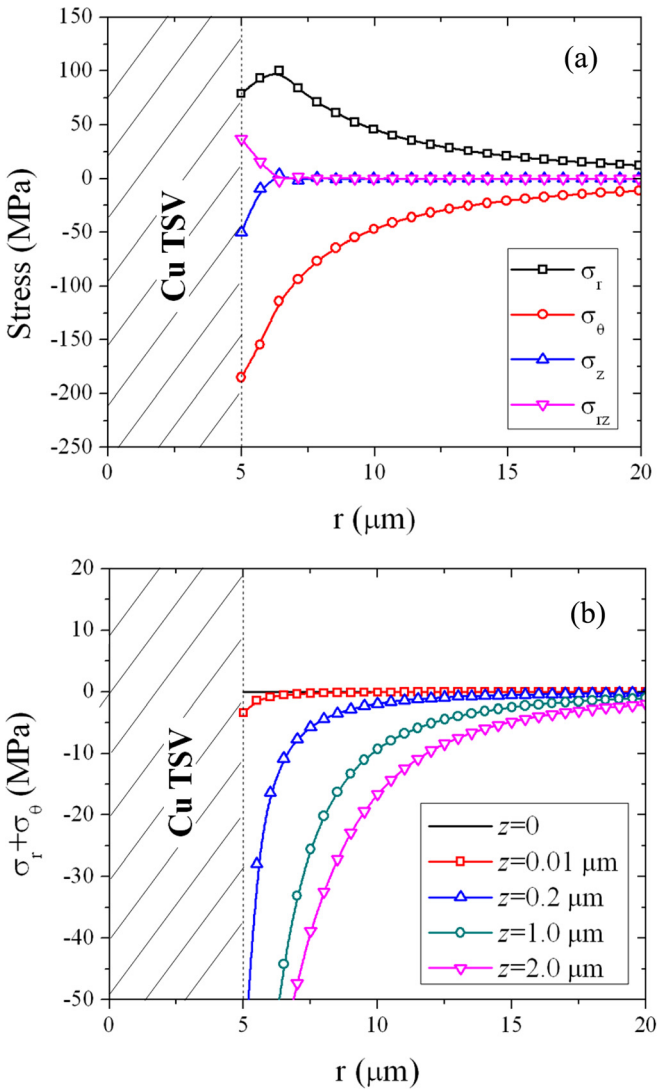

FIG. 2. Near-surface stresses around an isolated TSV predicted by the semi-analytical solution ($\Delta T = -100\,^{\circ}\mathrm{C}$ and $D = 10\,\mu$m). (a) Stress components at $z = 0.2\ \mu$m; (b) sum of the in-plane normal stresses at different depths.

With Eqs. (4) and (5), the sum of the radial and circumferential stresses is obtained as

$$\sigma_r + \sigma_\theta = \frac{-E\varepsilon_T}{2\pi(1-\nu)} \int_0^{\frac{D}{2}} \int_0^{2\pi} \left(\frac{3z^3}{R^5} - \frac{2(1+\nu)z}{R^3} \right) \rho \, d\rho \, d\theta \,. \quad (8)$$

It is found that, while the stress sum is identically zero both at the wafer surface ($z = 0$) and far away from the surface ($z \to \infty$), it varies with the depth (z) in the near-surface region as shown in Fig. 2(b). The stress sum is negative everywhere for $z > 0$ and $r > D/2$, whereas the magnitude decays monotonically as r increases and diminishes far away from the via. Since the two stress components have opposite signs as shown in Fig. 2(a), the magnitude of their sum is relatively small. Near the wafer surface ($z < 2$ μm), the magnitude of the stress sum increases with increasing depth. This suggests that the Raman signal depends on the laser penetration depth, which in turn depends on the laser wavelength.[28] On the other hand, while the stress magnitude is increasingly high approaching the Si/TSV interface, the Raman signal as shown in Fig. 1(b) becomes noisy due to the reduction in the Raman intensity. Thus, the Raman data very close to the interface shall be interpreted with caution.

Next, we lift the two major assumptions made in the semi-analytical solution by numerical analyses based on the finite element method. First, the heterogeneous materials in the TSV structure are considered with different elastic moduli for the via material and the oxide layer, both taken to be linear elastic and isotropic, with $E_f = 110$ GPa and $\nu_f = 0.35$ for the Cu via, and $E_o = 70$ GPa and $\nu_o = 0.16$ for the oxide layer. The thin Ta layer on the sidewall has negligible effect on the stress state in Si, thus ignored in the finite element analysis (FEA). Second, the elastic anisotropy of Si is taken into account by using the anisotropic elastic constants for Si crystal.[29] A three-dimensional model is constructed using the commercial finite-element package, ABAQUS (v6.8). As shown in Fig. 3(a), the FEA model consists of three different materials (Cu, oxide, and Si), without the surface oxide layer; the effect of surface oxide layer is discussed in the next section. To simulate the periodic TSV array used for the Raman measurements, symmetric boundary conditions are applied to the side faces in [110] and [$1\bar{1}0$] directions with different pitch distances (40 and 50 μm, respectively). Furthermore, by symmetry, only a quarter of the via is modeled. To further reduce the computational model size, the wafer thickness is taken to be 100 μm in the FEA model instead of 700 μm in the real specimen, while the TSV depth is 55 μm. The top surface is traction free, and the out-of-plane displacement (z-direction) at the bottom surface is set to be zero. With such a boundary condition, increasing the wafer thickness has negligible effect on the near-surface stress distribution. Linear 3D solid elements (C3D8R) are used, with a relatively fine mesh near the wafer surface (element size = 0.1 μm in the thickness direction and 0.2 μm in the lateral direction) and an increasingly coarse mesh away from the surface and TSV.

The contours of the stress sum, $\sigma_r + \sigma_\theta$, calculated at the depth $z = 0.2$ μm are shown in Figs. 3(b) and 3(c). For comparison, Fig. 3(b) shows the result from an isotropic Si model with $E_m = 130$ GPa and $\nu_m = 0.28$, where the stress field is axi-symmetric with concentric circular contours for the stress sum. Unlike the results for an isolated TSV shown in Fig. 2(b), the stress sum in Si becomes positive except for the regions very close to the via, due to the interaction between neighboring vias in the periodic array. Using the anisotropic elastic property for the (001)Si, the stress distribution as shown in Fig. 3(c) exhibits a four-fold symmetry, reflecting the cubic symmetry of the Si crystal. Due to the

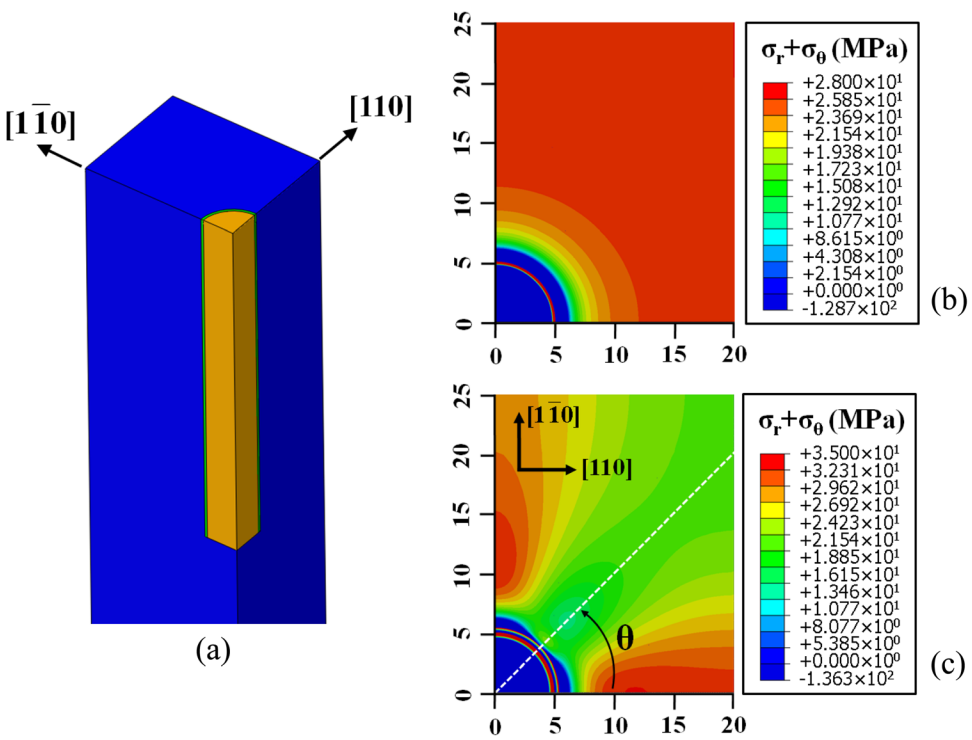

FIG. 3. (a) Part of the 3D FEA model showing a quarter of the Cu via (orange) embedded in Si (blue) along with a thin oxide layer (green) at the interface. (b) and (c) Show distributions of the stress sum ($\sigma_r + \sigma_\theta$) near the wafer surface ($z = 0.2$ μm) for an isotropic Si model and an anisotropic (001) Si wafer, respectively.

different pitch distances in the [110] and [$1\bar{1}0$] directions, the stress variation is slightly different in the two directions. This result suggests that, due to the elastic anisotropy of Si and the via−via interactions, the near-surface stress measured by Raman spectroscopy could depend on the direction of Raman scanning. To quantitatively examine the directional dependence of the Raman signal for the (001) Si wafer, we show in Fig. 4 the stress sum along different directions of line scanning, by varying the angle θ from the [110] direction. In particular, we note that, along the [110] direction ($\theta = 0^\circ$), the magnitude of the stress sum reaches a positive peak at $r \sim 10\mu$m. The magnitude of the positive peak stress is around 30 MPa. A previous study has reported qualitatively similar variation of the stress by Raman measurements, but with a higher positive peak stress (~50 MPa).[15] Among all the directions shown in Fig. 4, relatively strong Raman signal is expected along the [110] direction. However, the difference among all angles is less than 20 MPa, close to the stress resolution for the Raman measurement. Thus it may be practically difficult to measure the directional dependency using the Raman spectroscopy.

V. DISCUSSION

A. Comparison between Raman and FEA results

Using Eq. (3), the measured Raman frequencies can be converted to the stress sum. To determine the reference frequency, ω_0, the Raman scans were not only performed between the vias but also extended to the bare silicon surface far away from the vias, where the stress sum is expected to be zero. As shown in Fig. 5(a), the average Raman frequency obtained from the far-field measurement gives the reference frequency, $\omega_0 = 520.39\,\text{cm}^{-1}$. For this measurement, the surface oxide layer on the TSV sample was mechanically polished, and the sample was subsequently subject to an anneal step at 200 °C. All the Raman measurements were conducted after cooling down to the room temperature.

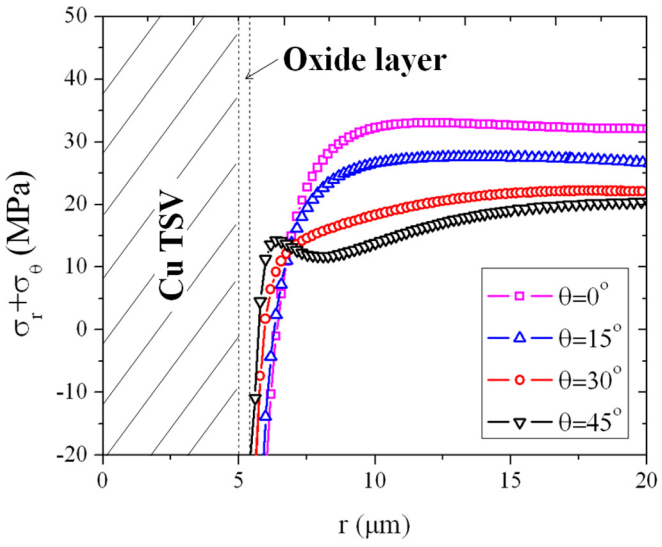

FIG. 4. Directional dependence of the stress distribution for (001) Si wafer ($\Delta T = -100\,^\circ$C, $D = 10\ \mu$m, and $z = 0.2\ \mu$m).

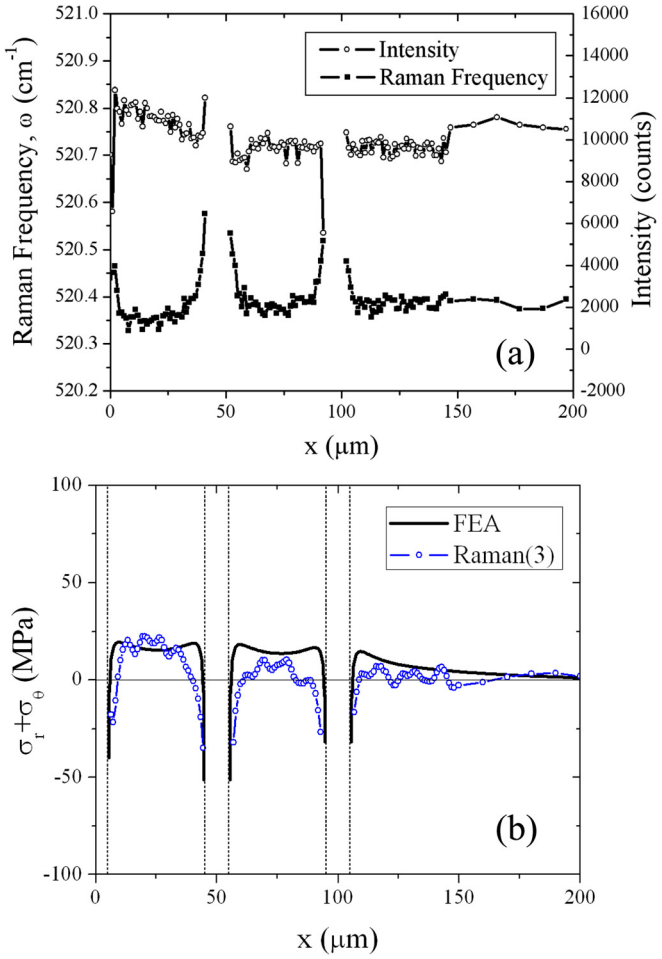

FIG. 5. (a) Measured Raman intensity and frequency for a TSV specimen with the surface oxide layer polished off. (b) Comparison of the near-surface stress distribution between Raman measurements and finite element analysis ($\Delta T = -70\,^\circ$C). Vertical dashed lines indicate the Cu/Si interfaces.

The Raman data in Fig. 5(a) is similar to those in Fig. 1(b) for the specimen with the surface oxide layer, but the frequency is slightly lower for the specimen without the surface layer. The effect of surface oxide layer is discussed further in the next section. In Fig. 5(b), we convert the measured Raman frequencies to stresses by Eq. (3) using $\omega_0 = 520.39\,\text{cm}^{-1}$, in comparison with the stresses obtained from the FEA model. For the FEA model, the materials are assumed to be linear elastic as described in Sec. IV. As a result, the stress magnitude from the FEA model depends linearly on the temperature change, ΔT, from the reference temperature to the room temperature (~30 °C). In a separate study using the bending beam technique,[26] the reference temperature for the TSV specimen was determined to be around 100 °C, and thus $\Delta T = -70\,^\circ$C for the Raman measurements. With $\Delta T = -70\,^\circ$C the results from the FEA model are in reasonable agreement with the Raman data as shown in Fig. 5(b). By taking into account the laser intensity attenuation, the stress obtained from the Raman measurement may be considered as a weighted volume average of the near-surface stress up to the laser penetration depth.[30] In the present study, the average stress calculated based on the FEA results was found to be close to the stress at $z = 0.2\ \mu$m, which is taken as the effective depth for the comparison. We

note that the stress magnitude is relatively low in this case due to small ΔT, which makes it difficult for the Raman measurement with the relatively large noise-to-signal ratio.

Additional Raman measurements were performed for the TSV samples annealed at 300 °C for 1 hour. In this case, stress relaxation by grain growth in the Cu vias was observed and the TSV specimen became nearly stress free at 300 °C as confirmed by the wafer curvature measurements.[26] Therefore, the thermal load was taken to be −270 °C in the FEA-based thermomechanical analysis. In Fig. 6, the stresses from the Raman measurements were compared to the FEA result with $\Delta T = -270$ °C. For the stress conversion, the same reference frequency ($\omega_0 = 520.39\,\text{cm}^{-1}$) was used. Compared to Fig. 5, the stress magnitude in Si has increased due to annealing at 300 °C, which raises the reference temperature for the induced thermal stresses upon cooling down to the room temperature. It is thus important to note that the near-surface stresses in the TSV structures as measured by Raman spectroscopy are process dependent due to the athermal contributions such as grain growth in the Cu vias, with important implications for the effect of process temperatures on the TSV reliability and device performance.

B. Effect of surface oxide layer

Recently, the via-middle approach has gained popularity for the TSV processing over the via-first or via-last. In this approach, processing of transistors is performed first, followed by the via patterning, oxide deposition, via filling with Cu, and chemical mechanical polishing (CMP) using oxide as a CMP stop.[31] This section is concerned with the effect of thin oxide layer from the via-middle process on the stresses developed at the buried silicon surface, where active components are located.

With an oxide layer on the wafer surface as illustrated in Fig. 1(a), the measured Raman frequencies in Fig. 1(b) were converted to stresses by Eq. (3), as shown in Fig. 7. Here, a different reference frequency was used ($\omega_0 = 521.44\,\text{cm}^{-1}$)

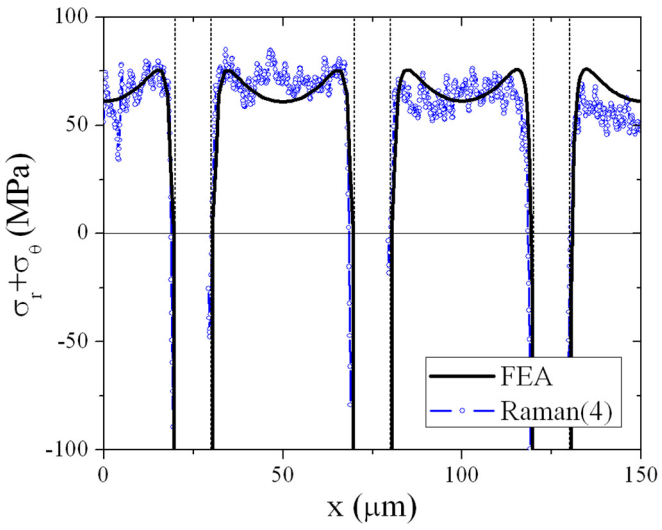

FIG. 6. Comparison of the near-surface stress distribution between Raman measurements and finite element analysis ($\Delta T = -270$ °C), for a TSV specimen annealed at 300 °C for 1 hour.

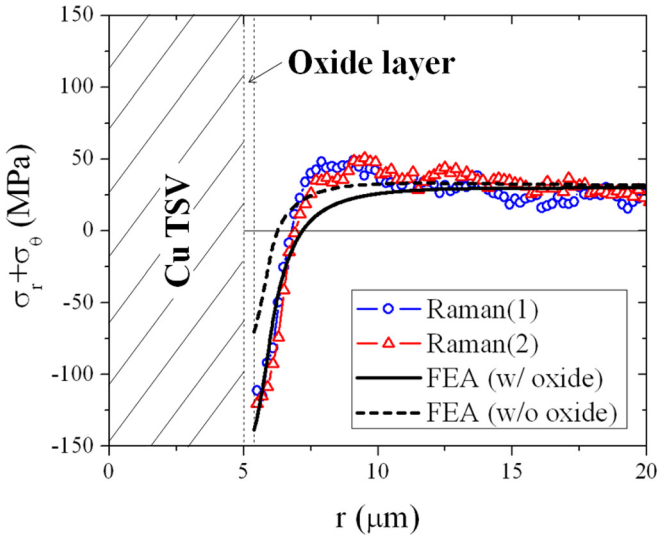

FIG. 7. Comparison of the near-surface stress distribution between Raman measurements and finite element analysis around a Cu TSV in (001) Si wafer with a surface oxide layer. Vertical dash lines indicate the Cu/barrier and barrier/Si interfaces.

since this measurement was performed using a different Raman system. The presence of the oxide layer is not expected to change the reference frequency. Assuming similar penetration depth (~0.2 μm) in Si, the stress state measured by Raman is at $z = 1.0$ μm from the wafer surface, which is slightly different from the case without the surface oxide layer. As shown in Fig. 7, with the surface oxide layer, the tensile stress is lower and the compressive stress is higher in Si, according to the FEA model ($\Delta T = -100$ °C). The FEA results compare closely with the Raman results except for a region with $7\ \mu\text{m} < r < 10\ \mu\text{m}$, where the Raman measurements have a peak tensile stress of around 50 MPa. Similar peak stresses were observed in a previous study.[15] The FEA model without the surface oxide layer does predict a peak tensile stress of similar magnitude (see Fig. 6). With the surface oxide layer, however, no peak stress is observed from the FEA model. The reason for such a discrepancy is unclear.

C. Effect of plasticity

The thermal stresses in the Cu vias may cause plastic deformation, which in turn may influence the stresses in Si. A finite element model is used to study the effect of plasticity in the metal vias. The classical metal plasticity model is adopted for the via material, with rate-independent perfect plasticity and a von-Mises yield surface for associated plastic flow. In addition to the elastic properties of Cu, the yield strength of Cu is specified in the FEA model. For electroplated Cu with the grain size of a few microns, previous studies[32] have found that the yield stress (σ_y) varies between 250 and 100 MPa. Figure 8 compares the result from the plastic FEA model with that from the previous model assuming all elastic materials. A relatively large thermal load, ΔT = -300 °C, is assumed in both models. A yield strength, σ_y = 200 MPa, is assumed for the Cu vias in Fig. 8(b). Apparently, plastic yielding leads to much large local deformation

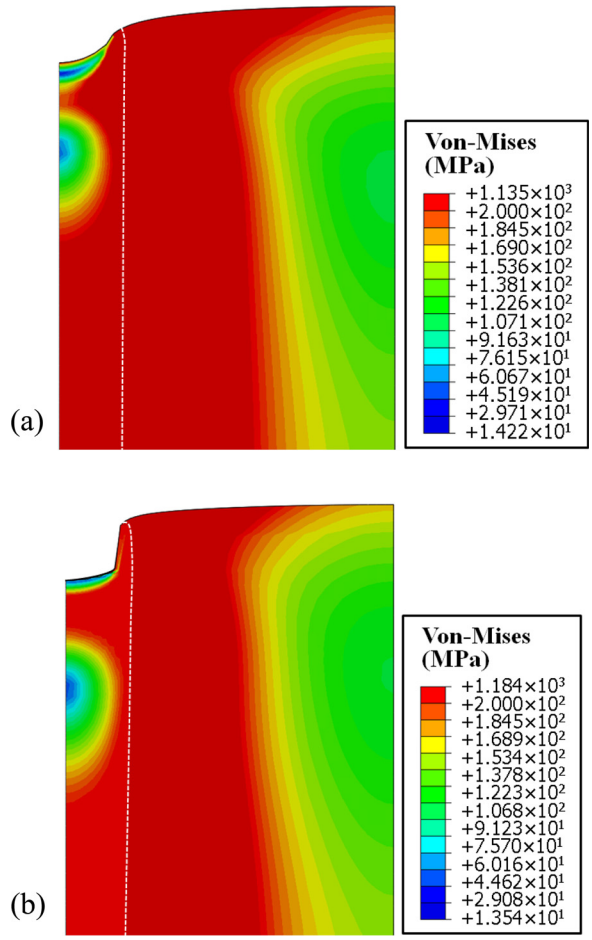

FIG. 8. Comparison of the elastic (a) and plastic (b) deformation near the wafer surface of a TSV structure by finite element analysis ($\Delta T = -300\,^{\circ}\mathrm{C}$).

of the via. The plastic deformation is largely confined to a relatively small region close to the junction of the Cu/via interface and the wafer surface, which causes the via surface to sink in significantly. Similarly, with a positive thermal load ($\Delta T > 0$), via extrusion is predicted due to the local plastic deformation. The phenomenon of via extrusion has been observed as a common failure mode for TSV structures.[26,33] The via extrusion could also result from interfacial delamination.[10] However, the local plasticity could reinforce the interfacial adhesion to prevent delamination,[34] while via extrusion can still occur due to plastic deformation.

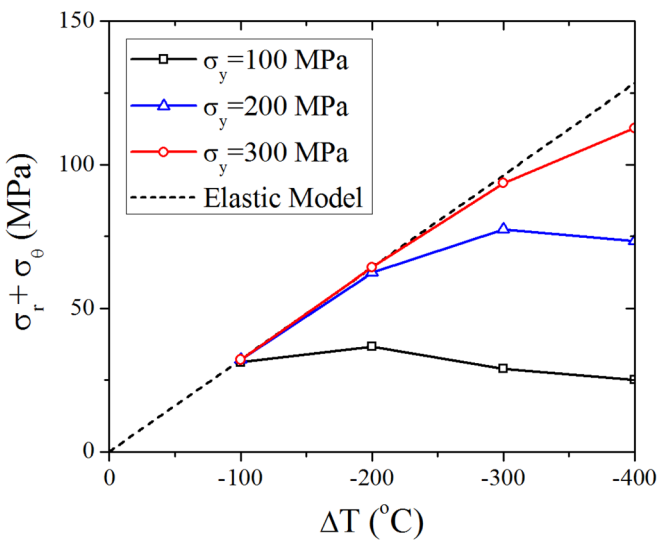

FIG. 9. Effect of Cu plasticity on the stress in Si ($r = 20$ μm and $z = 0.2$ μm).

As a result of the local plasticity, the stress in Si around the via changes slightly near the interface but not much elsewhere. Figure 9 plots the stress in Si at $r = 20$ μm as a function of the temperature change, comparing the results from the all-elastic model and three elastic-plastic models with different yield strengths. The stress in Si increases linearly with the temperature change in the all-elastic model. With plastic deformation in the via, the stress deviates from the linear behavior, depending on the yield strength. In addition to the plastic deformation, grain growth in the metal vias has been observed during thermal cycling,[26] which could relax the thermal stress in the vias and thus further reduce the stress in Si.

VI. SUMMARY

In summary, micro-Raman measurements of the near-surface stresses in a TSV structure are presented along with detailed stress analyses based on a semi-analytic approach and finite element analysis. In particular, the depth dependence of the stress distribution and the effect of elastic anisotropy of Si are elucidated for properly interpreting the Raman data. A reasonable agreement between the Raman measurements and the finite element analysis is obtained for the TSV specimen without the surface oxide layer. The effects of the surface oxide layer and metal plasticity of the via material on the stress and Raman measurements are discussed. The results from the present study suggest that micro-Raman spectroscopy is a viable approach to characterize the local stresses in the integrated TSV structures, along with detailed stress analysis.

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[1]International Technology Roadmap for Semiconductors (ITRS) (2009).
[2]L. W. Schaper, S. L. Burkett, S. Spiesshoefer, G. V. Vangara, Z. Rahman, and S. Polamreddy, IEEE Trans. Adv. Packag. **28**, 356–366 (2005).
[3]J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, M. J. Interrante, C. S. Patel, R. J. Polastre, K. Sakuma, R. Sirdeshmukh, E. J. Sprogis, S. M. Sri-Jayantha, A. M. Stephens, A. W. Topol, C. K. Tsang, B. C. Webb, and S. L. Wright, IBM J. Res. Dev. **52**, 553–569 (2008).
[4]J.-Q. Lu, Proc. IEEE **97**, 18–30 (2009).
[5]N. Ranganathan, K. Prasad, N. Balasubramanian, and K. L. Pey, J. Micromech. Microeng. **18**, 075018 (2008).
[6]C. S. Selvanayagam, J. H. Lau, X. Zhang, S. K. W. Seah, K. Vaidyanathan, and T. C. Chai, IEEE Trans. Adv. Packag. **32**, 720–728 (2009).
[7]X. Liu, Q. Chen, P. Dixit, R. Chatterjee, R. Tummala, and S. Sitaraman, *Proc. Electronic Components and Technology Conference*, pp. 624–629 (IEEE, Piscataway, 2009).
[8]K. H. Lu, X. Zhang, S. K. Ryu, J. Im, R. Huang, and P. S. Ho, *Proc. Electronic Components and Technology Conference* (IEEE, Piscataway, 2009), pp. 630–634.

[9]K. H. Lu, S. K. Ryu, Q. Zhao, X. Zhang, J. Im, R. Huang, and P. S. Ho, *Proc. Electronic Components and Technology Conference* (IEEE, Piscataway, 2010), pp. 40–45.
[10]S. K. Ryu, K. H. Lu, X. Zhang, J. H. Im, P. S. Ho, and R. Huang, IEEE Trans. Device Mater. Reliab. **11**, 35–43 (2011).
[11]S. Thompson, G. Sun, Y. Choi, and T. Nishida, IEEE Trans. Electron Devices **53**, 1010–1020 (2006).
[12]A.P. Karmarker, X. Xu, and V. Moroz, *Proc. IEEE 47th Annual International Reliability Physics Symposium* (IEEE, Piscataway, 2009), pp. 682–687.
[13]M. Hecker, L. Zhu, C. Georgi, I. Zienert, J. Rinderknecht, H. Geisler, and and E. Zschech, AIP Conf. Proc. **931**, 435–444 (2007).
[14]C. Okoro, Y. Yang, B. Vandevelde, B. Swinnen, D. Vandepitte, B. Verlinden, and I. De Wolf, *Proc. IEEE International Interconnect Technology Conference* (IEEE, Piscataway, 2008), pp. 16–18.
[15]C. McDonough, J. Capulong, B. Backes, P. Singh, L. Smith, W. Wang, and R. E. Geer, SEMATECH Workshop on Stress Management for 3D ICs (2010).
[16]Q. Ma, S. Chiras, D. R. Clarke, and Z. Suo, J. Appl. Phys. **78**, 1614–1622 (1995).
[17]I. De Wolf, Semicond. Sci. Technol. **11**, 138–154(1996).
[18]D. J. Gardiner, *Practical Raman Spectroscopy* (Springer-Verlag, New York, 1989).
[19]F. Cerdeira, C. J. Buchenauer, F. H. Pollak, and M. Cardona, Phys. Rev. B **5**, 580–593 (1972).
[20]B. Wang, M. A. Dündar, A. Y. Silov, R. Notzel, F. Karouta, S. He, and R. W. van der Heijden, Opt. Lett. **35**, 2603–2605 (2010).
[21]A. Chandrasekhar, J. B. Renucci, and M. Cardona, Phys. Rev. B **17**, 1623–1633 (1978).
[22]E. Anastassakis, A. Cantarero, and M. Cardona, Phys. Rev. B **41**, 7529–7535 (1990).
[23]V. T. Srikar, A. K. Swan, M. SelimÜnlü, B. B. Goldberg, and S. M. Spearing, J. Microelectromech. Syst. **12**, 779–787 (2003).
[24]J. Chen and I. De Wolf, IEEE Trans. Compon. Packag. Technol. **28**, 484–492 (2005).
[25]R. P. Koseski *et al.*, J. Appl. Phys. **110**, 073517 (2011).
[26]S. K. Ryu, T. Jiang, K. H. Lu, J. Im, H.-Y. Son, K.-Y. Byun, R. Huang, and P. S. Ho, Appl. Phys. Lett. **100**, 041901 (2012).
[27]T. C. Lu, J. Yang, Z. Suo, A. G. Evans, R. Hecht, and R. Mehrabian, Acta Metall. Mater. **39**, 1883–1890 (1991).
[28]A. D. Trigg *et al.*, Appl. Phys. Express **3**, 086601 (2010).
[29]J. J. Wortman and R. A. Evans, J. Appl. Phys. **36**, 153–156 (1965).
[30]I. De Wolf, H. E. Maes, and S. K. Jones, J. Appl. Phys. **79**, 7148–7156 (1996).
[31]P. Garrou and C. Bowen, *Handbook of 3D Integration* (Wiley-VCH, 2008), Vol. **1**, pp. 25–43.
[32]Y. Xiang, T. Y. Tsui, and J. J. Vlassk, J. Mater. Res. **21**, 1607–1618 (2006).
[33]L. W. Kong, A. C. Rudack, P. Krueger, E. Zschech, S. Arkalgud, and A. C. Diebold, Microelectron. Eng. **92**, 24–28 (2012).
[34]M. J. Cordill, N. R. Moody, and D. F. Bahr, Acta Mater. **53**, 2555–2562 (2005).