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Delamination in Patterned Films

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Abstract

When the dielectric constant of an insulator in an interconnect is reduced, mechanical properties are often compromised, giving rise to significant challenges in interconnect integration and reliability. Due to low adhesion of the dielectric an interfacial crack may occur during fabrication and testing. To understand the effect of interconnect structure, an interfacial fracture mechanics model has been analyzed for patterned films undergoing a typical thermal excursion during the integration process. It is found that the underlayer pattern generates a driving force for delamination and changes the mode mixity of the delamination. The implications of our findings to interconnect processes and reliability testing have been discussed.

1 Introduction

To perform electronic functions, CMOS transistors are wired by multiple levels of metal lines that are connected through vias from one level to another. The metal lines are insulated by dielectric. The fabrication of the wiring is called back-end-of-line (BEOL) process, which builds the interconnect structures on top of transistors. An important gauge for BEOL performance is RC, which is the electrical resistance of the metal lines times the capacitance of the wiring. By reducing RC the chip performance can be improved, the chip power can be lowered and the cross talk between neighboring lines can be reduced. RC depends on the interconnect structures and the materials used in BEOL. One way to reduce RC is by optimizing BEOL design and the other is to adopt new materials. For many decades aluminum and oxide have been used for the conductor and insulator, respectively. To reduce the resistance the microelectronics industry first replaced aluminum with copper (Edelstein et al, 1997, where BEOL has also been scaled to reduce capacitance), and then substituted oxide with low dielectric constant (low-k) insulator to reduce capacitance.

[1] Dedicated to the Sixtieth Birthday of Professor Choon Fong Shih
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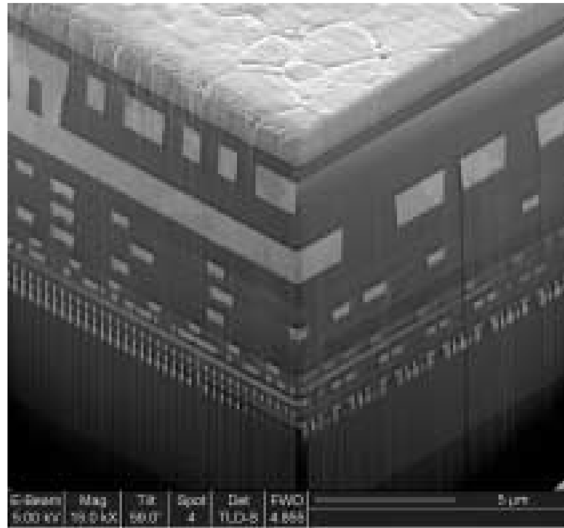

Fig. 1. Copper and low-k interconnect structures in IBM CMOS microprocessor (Edelstein et al, 2004)

Figure 1 shows IBM's 90nm microprocessor chip with eight levels of copper wiring integrated into SiCOH low-k dielectric (Edelstein et al, 2004). The introduction of low-k material into CMOS products has been achieved by solving many fundamental problems in physics and chemistry. For many low-k dielectrics one of the critical issues was the weak mechanical properties. In terms of the modulus, fracture toughness and adhesion of low-k dielectric to other materials used in BEOL, low-k dielectrics have lower values than oxide. They are tensile films after deposition rather than compressive as with oxide, making them more susceptible to cracking. Such a weakness in mechanical properties poses significant challenges to copper/low-k integration and BEOL reliability. As the industry is moving to reduce dielectric constant, for example, by incorporating pores into the dielectric, the mechanical properties become worse. It is therefore important to understand the basic issues regarding to mechanical stability of interconnect structures during integration and reliability testing.

When a dielectric deposited on a silicon substrate is too fragile, it fails cohesively, resulting in channel cracking. The mechanics of channel cracking has been studied extensively, as documented in the review by Hutchinson and Suo in 1992. Since then, many aspects that affect the driving force have been published in literature, for example, the inelastic material behavior such as plasticity (Beuth and Klingbeil, 1996) and viscosity (Suo, Prévost and Liang, 2003), and the enhancement of the energy release rate due to the metal pattern (Ambrico, Jones and Begley, 2002, Liu et al, 2004).

When a blanket film is deposited on a wafer with patterned film, the energy

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release rate of channel cracking is increased significantly by the copper pattern underneath (Ambrico, Jones and Begley, 2002). Fig. 2 shows the interconnect structure for which the enhancement of the energy release rate has been calculated and verified by experiment (Liu et al, 2004). The energy release rate G has been normalized by G_0, the driving force for a blanket low-k film directly on silicon substrate. It is clear in Fig. 3 that the energy release rate depends on the width of the gap between the copper pads. At some gap spacing the energy release rate attains a maximum that can be an order higher than the case without a patterned underlayer.

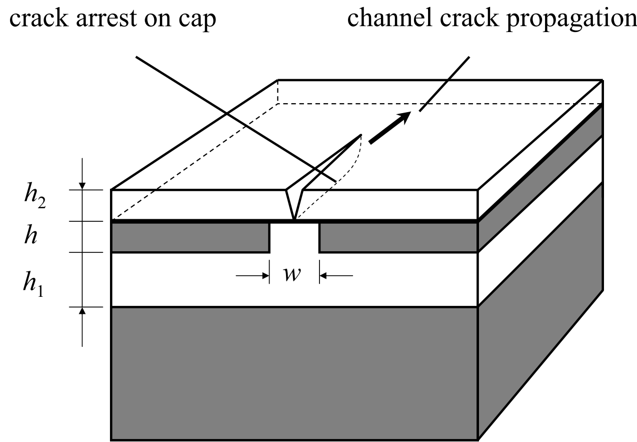

Fig. 2. Channel crack in a film on patterned underlayer.

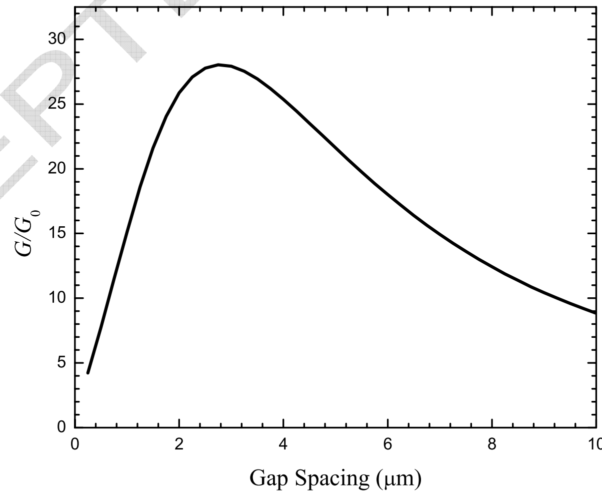

Fig. 3. Energy release rate for a channel crack in Fig. 2 with $h = h_1 = w = 1\mu m$ and $h_2 = 0.5\mu m$ (Liu et al, 2004)

When adhesion of low-k dielectric to other materials in BEOL is too low,

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delamination can occur at the interfaces. Many unit processes of BEOL fabrication, such as film deposition of low-k dielectric, involves high temperature. At room temperature the BEOL multiple levels of interconnect structures have residual stress due to the thermal expansion mismatch, elastic mismatch and complicated wring. The energy release rate for a channel crack is sensitive to the underlayer pattern as described before. It is of interest to understand whether an interracial cracking depends on the underlayer metal pattern or not. In the reliability test of thermal cycling a packaged chip undergoes temperature cycles to determine if it can pass a number of cycles specified by the industry standard. It is unclear if the residual stress in BEOL contributes to interfacial cracking in the test. In this paper a fracture mechanics model is analyzed to study the effects of BEOL patterns on the energy release rate for delamination, aiming to resolve the above questions for copper/low-k integration and reliability testing.

2 Interfacial Fracture Mechanics

Interfacial fracture mechanics has been well established in the nineteen nineties both theoretically and experimentally. It is a classical problem in fracture mechanics that was re-ignited by interest in modern engineering applications, in particular the microelectronics industry. Here we only outline the concepts and the results that will be used in our discussion. The reader may refer to the review articles for more detail (Rice 1988, Shih 1991, and Hutchinson and Suo, 1991)

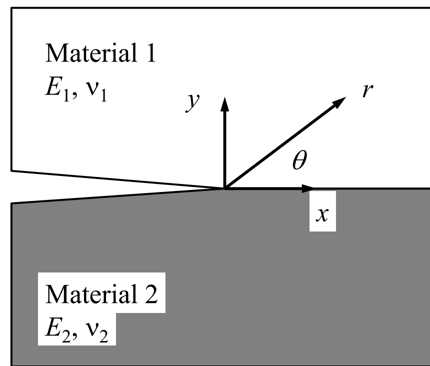

Fig. 4. Interface crack and notation

Figure 4 shows the notation for an interface crack between materials 1 and 2. The elastic constants are the Young's modulus E and Poisson's ratio ν with a

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subscript 1 and 2, respectively, for each material. The stress field in the crack tip region can be represented asymptotically by the following form,

$$\sigma_{ij} = \frac{\mathrm{Re}[Kr^{i\varepsilon}]}{\sqrt{2\pi r}}\tilde{\sigma}_{ij}^{\mathrm{I}}(\theta,\varepsilon) + \frac{\mathrm{Im}[Kr^{i\varepsilon}]}{\sqrt{2\pi r}}\tilde{\sigma}_{ij}^{\mathrm{II}}(\theta,\varepsilon). \tag{1}$$

Here i in the power function of r is the imaginary number, and the subscript, ij, stands for the component of stress. Re and Im are the real and imaginary part of the complex arguments, and r and θ are defined in Fig. 4. The angular functions $\tilde{\sigma}_{ij}^{\mathrm{I}}$ and $\tilde{\sigma}_{ij}^{\mathrm{II}}$ are normalized (Rice, Suo and Wang, 1990) such that at the interface $\theta = 0$ and the traction reduces to

$$\sigma_{yy} + i\sigma_{yx} = \frac{Kr^{i\varepsilon}}{\sqrt{2\pi r}}. \tag{2}$$

The index ε is defined by,

$$\varepsilon = \frac{1}{2\pi}\ln\left(\frac{1-\beta}{1+\beta}\right), \tag{3}$$

where β is one of the Dundur's elastic mismatch parameters and is related to the shear modulus $\mu = E/2(1+\nu)$. With $\kappa = 3 - 4\nu$ for plane strain β takes the following from,

$$\beta = \frac{\mu_1(\kappa_2 - 1) - \mu_2(\kappa_1 - 1)}{\mu_1(\kappa_2 + 1) + \mu_2(\kappa_1 + 1)}. \tag{4}$$

In Eq. (1) the complex stress intensity factor is given by $K = K_1 + iK_2$ with K_1 and K_2 analogous to the conventional stress intensity factors K_{I} and K_{I}. However, in interfacial fracture mechanics, the tensile and shearing modes are inseparably coupled due to the elastic mismatch when ε is not zero. The mode mixity, a measure of shear relative to tension at the interface, can be defined by,

$$\tan\psi = \frac{\mathrm{Im}(KL^{i\varepsilon})}{\mathrm{Re}(KL^{i\varepsilon})} \tag{5}$$

where L is a fixed length for a material pair (Rice 1988, Shih 1991).

Instead of the complex stress intensity factor K, the driving force to propagate an interface crack can also be represented by the energy release rate $\mathcal{G}$ which is given by,

$$\mathcal{G} = \frac{1-\beta^2}{E^\star}|K|^2, \tag{6}$$

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where

$$\frac{1}{E^\star} = \frac{1}{2}\left(\frac{1}{\bar{E}_1} + \frac{1}{\bar{E}_2}\right). \tag{7}$$

Here $\bar{E} = E/(1-\nu^2)$ for plane strain. In a form similar to the stress in Eq. 2 the relative displacement of the crack surfaces is asymptotically specified by the complex stress intensity K,

$$\delta = \delta_y + i\delta_x = \frac{1}{(1+2i\varepsilon)\cosh(\pi\varepsilon)} \frac{4Kr^{i\varepsilon}}{E^\star}\sqrt{\frac{2r}{\pi}}. \tag{8}$$

To determine the driving force for an interfacial crack one needs to solve a boundary value problem to obtain the complex stress intensity K, or equivalently, the energy release rate $\mathcal{G}$ plus the mode mixity ψ. In this paper we choose the latter pair of parameters to characterize the driving force for delamination in patterned films. The boundary value problem is solved using the finite element model described in the following section.

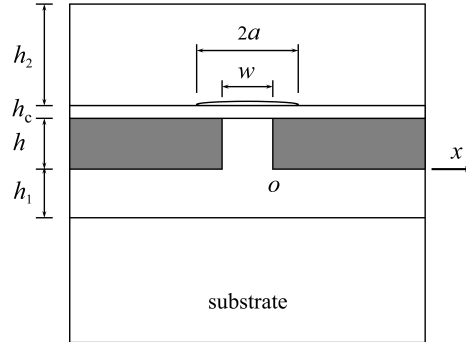

Fig. 5. Geometry of patterned underlayer and delamination

3 Finite Element Model

Figure 5 shows the representative geometry of the thin film structure studied in our work. It has one patterned film under blanket films. The shaded areas are two semi-infinite copper plates with a thickness h and a gap w between them. The copper plates are embedded in low-k dielectric with low-k of thickness h_1 beneath them. The patterned film is capped by a layer of thickness h_c, and on top of it is the second layer of low-k of thickness h_2. A delamination of length $2a$ is inserted between the cap and the low-k dielectric above. When the second low-k layer is deposited and before it is patterned, the whole structure has undergone a thermal excursion from a high temperature of deposition to

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Table 1
Thermo-mechanical properties of materials

Material	E (GPa)	ν	CTE (ppm/°C)
Si	169	0.28	3
Cu	130	0.34	16.5
SiCN	100	0.3	3
low-k	10	0.3	11

room temperature. It is noted that in addition to the cap there are Ta based liners enclosing the wiring lines to prevent the copper atoms from diffusing into the dielectric (Edelstein et al, 2001). The liners are thin compared to the lines. To examine the delamination between low-k and cap it suffices to include the cap layer and neglect the liners. Unless stated otherwise the dimensions used in the calculations are $h = 1\mu m$, $h_1 = h$, $h_2 = 2h$, $h_c = h/5$ and $w = h$. The Young's modulus E, Poisson's ratio ν and coefficient of thermal expansion (CTE) are listed in Table 1, where SiCN is an insulator for the cap. For the low-k and SiCN material pair one has $\beta = -0.23$ and $\varepsilon = 0.076$.

Three levels of finite element meshes are constructed to discretize the geometry. At the first level a structured mesh of eight-node quadratic elements is used for the substrate and each blanket film in Fig. 6 (a). To simulate a thick substrate its length and width are chosen to be at least eighty times the total film thickness, gap spacing or delamination size. The cut-out region in Fig. 6 (a) is refined by an unstructured mesh of six-node triangular elements as shown in Fig. 6 (b). At this level the gap between the copper plates has been included while the crack region is refined at the next level in Fig. 6 (c) using unstructured six-node triangular elements. The region in the last level contains the inter-level dielectric (ILD), the cap and the delamination in Fig. 6 (c). It can be placed at any location along the low-k and cap interface so that the position of the delamination can be varied relative to the gap. In Fig. 6 (c) a ring of triangular elements are concentrated at the crack tip and their mid-side nodes are shifted to the quarter points to capture the $1/\sqrt{r}$ singularity in strain. Mesh generation is automated in the commercial finite element package by programming in APDL language so that parametric studies can be done by changing the dimensions of structure and delamination.

The interest of our study is to examine the delamination during BEOL processing. The driving force comes from the thermal mismatches between all the materials in the structure when temperature changes from deposition at 400° to 25°. In our calculations the the rigid body motion is removed by constraining the external boundaries of the finite element model except the top surface. In our calculations all the elements are in plane strain and the thermal ex-

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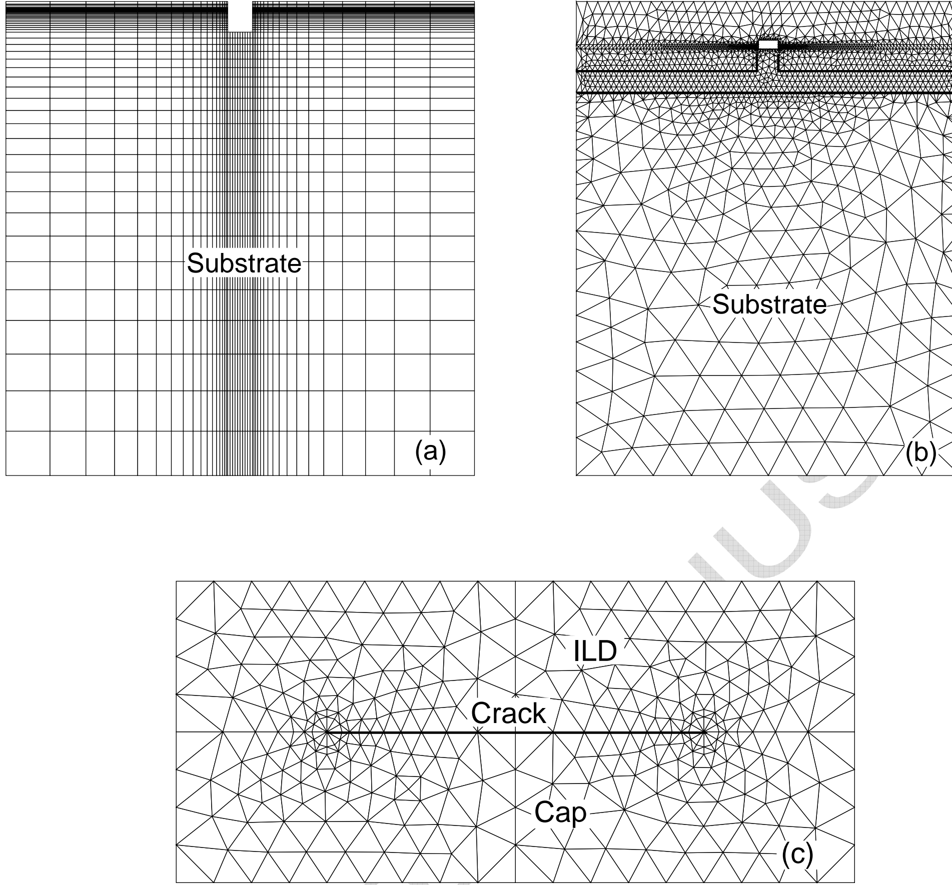

Fig. 6. Finite element meshes (a) mesh at global level (b) local mesh in global one (c) mesh for interfacial crack

pansion coefficient of each material is specified as the difference between the material and silicon.

To compute the energy release rate $\mathcal{G}$ a modified crack surface displacement method (Matos et al, 1989) is used. Eliminating K from Eq. (8) and (6) one has

$$\ln|\delta| = \ln\left[4\sqrt{\frac{2}{\pi(1+4\varepsilon^2)}\frac{\mathcal{G}}{E^\star}}\right] + \frac{1}{2}\ln r, \tag{9}$$

where the connection $1-\beta^2 = 1/\cosh^2(\pi\varepsilon)$ has been used. Therefore, when the crack surface displacements are solved from the finite element calculation, one can obtain the energy release rate by fitting the logarithmic δ vs. r data points in the K-controlled zone at the crack tip.

From Eq. (5) the relation between the phase angle ψ of mode mixity and that

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of K is,

$$\psi = \tan^{-1}\frac{K_2}{K_1} + \varepsilon \ln h_c, \tag{10}$$

where the cap thickness h_c is used for the length L. From Eq. (8) for the crack surface displacement one has,

$$\tan^{-1}\frac{\delta_x}{\delta_y} = \tan^{-1}\frac{K_2}{K_1} + \varepsilon \ln r - \tan^{-1} 2\varepsilon. \tag{11}$$

Eliminating the phase angle of K from the two equations yields

$$\psi = \tan^{-1}\frac{\delta_x}{\delta_y} + \varepsilon \ln \frac{h_c}{r} + \tan^{-1} 2\varepsilon, \tag{12}$$

which is used to compute the phase angle of mode mixity from the finite element results of the crack surface displacements.

4 Numerical Results

First it is noted that for a *blanket* film stack the energy release rate for any interfacial defect is zero, because the thermal mismatch only generates biaxial stress in the defect plane and no strain energy can be released by delamination. Indeed when a delamination is placed away from the gap in our model, the energy release rate obtained from the finite element calculation is zero. In contrast, when the film is patterned, such that a gap exists between the copper plates as in the model, there *is* a driving force for delamination. By varying the size of the crack at the low-k and cap interface and changing the location of the crack, it is found that the worst case occurs when the crack is within the gap. At other positions the energy release rate is lower or the crack closes. All the results are presented in the paper are for a crack centered at the gap and for the right crack tip.

It is well known that the energy release rate depends on the crack size. For example, the exact solution was solved (Rice and Sih, 1965) for a crack of size $2a$ at the interface of two infinite mediums. The solution for K and $\mathcal{G}$ are, respectively,

$$K = \sigma(1 + 2i\varepsilon)\sqrt{\pi a}(2a)^{-i\varepsilon}, \tag{13}$$

$$\mathcal{G} = \frac{(1-\beta^2)(1+4\varepsilon^2)}{E^\star}\pi\sigma^2 a. \tag{14}$$

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It is noted that the energy release rate increases to the square of the stress normal to the interface and it is linear in the crack length $2a$. In a patterned film the energy release rate also depends on the crack length as shown in Fig. 7. When the underlayer pattern is fixed, for example, the curve for $w/h = 1$, the energy release rate increases initially with the crack length, peaks at some length, decreases and climbs up to a steady state value at large crack lengths.

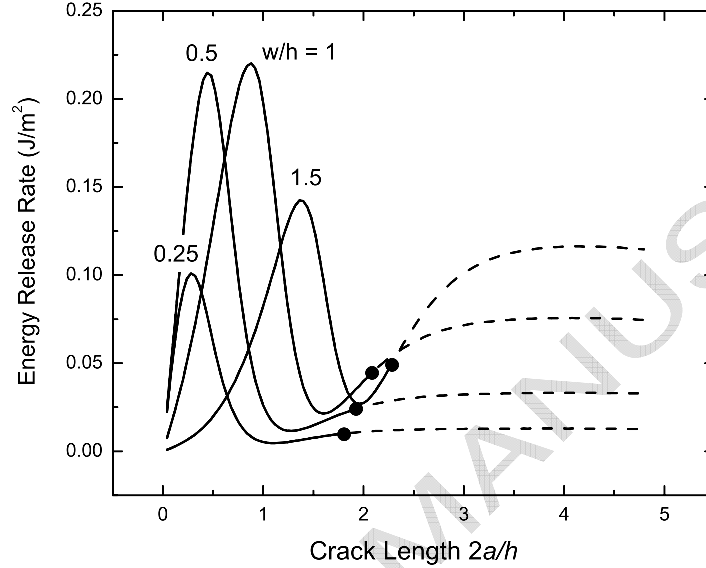

Fig. 7. Energy release rate as a function of delamination for different gap width

It is noted that for a small crack the results for the energy release rate agree with Eq. (14) when the local stress normal to the low-k and cap interface at the center of the gap is used. As the delamination grows the energy release rate increases. It peaks when the crack tip approaches the copper underlayer. This is because copper has the largest CTE in all the materials and it is stiff such that the stress concentrates at the the triple junction of copper, cap and low-k dielectric, resulting in a high energy density.

Figure 7 also includes the curves for different gap width w/h. The energy release rate strongly depends on the gap. In particular, the peak value of the energy release rate is lower for small or large gap width. It is maximized at some intermediate gap spacing. It is noted that the steady state energy release rate also depends on the gap width. Indeed, the steady state value $\mathcal{G}_{ss}$ is simply determined by the difference of strain energy far ahead of the crack, U_1 and that at the center of the gap, U_2. The former energy, U_1, is independent of the gap width. It is the sum of the strain energy per area for each film in the blanket state. The latter strain energy, U_2, at the center of the gap, depends on the gap spacing. When the temperature decreases, copper shrinks. The copper plates pull the low-k material in the gap. The larger the gap spacing, the smaller the energy stored and the smaller U_2. This leads to

the larger steady state value with the larger gap width from the difference $\mathcal{G}_{ss} = U_1 - U_2$.

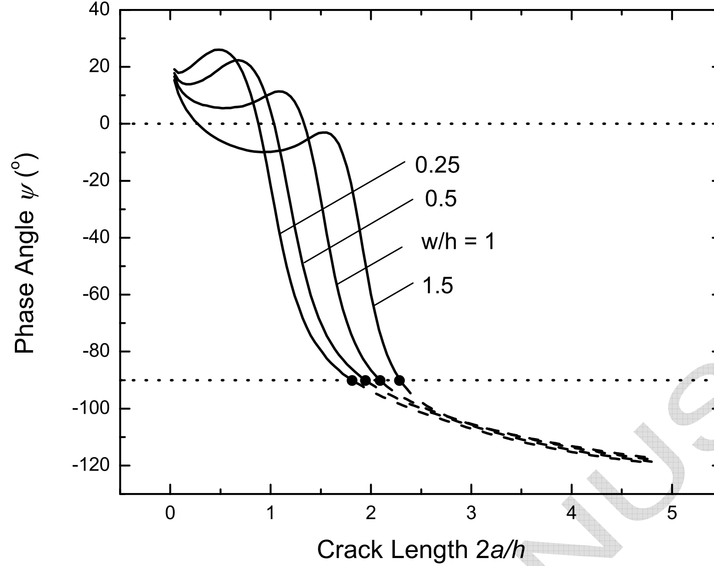

Fig. 8. Variation of the angle of mode mixity for the right tip of interfacial crack

For each curve in Fig. 7 the corresponding phase angle of mode mixity is plotted in Fig. 8 as a function of crack length. It is noted that the mode mixity varies significantly with delamination length. By the definition of the mode mixity the angles in the first and fourth quadrants indicate crack opening with positive and negative shear, respectively. Those angles in the second and third quadrants mean that the crack closes. In Fig. 8 all the curves starts with opening crack and positive shear at small delamination length. As the delamination grows the shear becomes negative. It is noted that the phase angle at very small crack length degenerates to the case of the exact solution (Rice and Sih, 1965). At large crack length the phase angle is less than $-90°$, indicating that the crack closes. A more sophisticated model may include surface contact, which will decrease the driving force for delamination. Since our focus is to find the worst case of the maximum driving force in pattern films, the calculations can be simply stopped when the phase angle is less than $-90°$ as indicated by solid circle data points shown in Fig. 7 and fig:ModeMixity. In all the subsequent figures the energy release rates are plotted only up to the point when crack closure occurs.

5 Deformation Analysis

Before undertaking parametric studies to examine pattern effects on delamination, it is useful to analyze the deformation of patterned films and confirm

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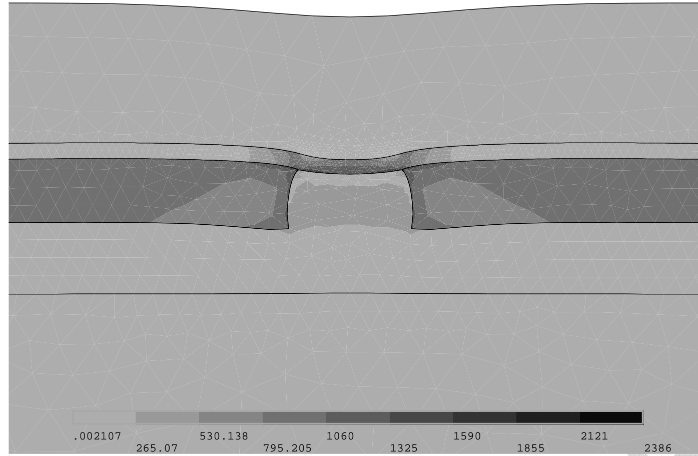

Fig. 9. Deformed shape and von Mises stress contour

the modeling by experimental techniques. It also helps to understand the remarkable pattern dependence of the energy release rate in Fig. 7 and the mode mixity in Fig. 8.

The analysis of the deformation is for the same structure in Fig. 5 and the mesh in Fig. 6, except that there is not an interface crack. Fig. 9 shows the deformation of the patterned film structure at room temperature. The deformed shape is magnified by 20× of the displacements, and on it the contour of von Mises stress is plotted. It is obvious that there is a stress concentration at the triple junction of copper, low-k and cap. It is remarkable that the cap bends concavely towards the substrate. This is from the thermal mismatch of copper that generates horizontal force that stretches the cap and bends it down, resulting in a tensile interfacial stress at the low-k and cap interface between the copper pads. Since the free surface deforms conformally with the cap, it is interesting to see if a measurement of surface profile gives the same result. A test structure similar to Fig. 5 but with more patterned films below the top blanket low-k film is fabricated. Atomic force microscopy (AFM) is used to scan the surface of the top blanket film. The profile obtained in Fig. 10 clearly shows the trough between two stacked copper pads, and validates the prediction by the finite element model.

Fig. 11 shows the stresses at the top low-k and cap interface. Because of symmetry only half of the interface to the right of the gap center ($x/w > 0$) is considered in our discussion. Between the copper pads ($|x/w| < 0.5$), the interface is in tension because the cap is pulled down by the patterned layer below. As the location moves from the gap to the copper pad, the normal stress changes from tension to compression. At some place on the interface

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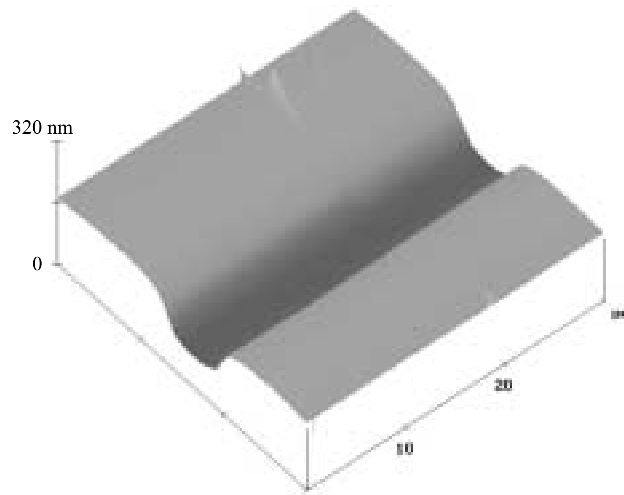

Fig. 10. Surface profile scanned by AFM measurements

there exists high compression and the normal stress increases to values of small tension and levels off to zero stress far away from the gap. With such a variation of the stress on the interface it is not surprising that the energy release rate varies with the crack length as shown in Fig. 7. In contrast to the normal stress, the shear stress changes from negative to positive shear inside the gap ($0 < x/w < 0.5$), and then follows the same trend of variation as the normal stress. It is noted that the mode mixity variation with the crack length in Fig. 8 correlates with the shear stress in Fig. 11. As the crack grows into the copper plate, the shear stress decreases quickly from positive to negative values, leading to the decreasing phase angle in Fig. 8. When the crack is within the gap, the phase angle of mode mixity first deceases and then increases due to the sign change in the shear stress.

6 Low-k Dielectrics and Multi-Level Structures

In this section other important aspects of the pattern are investigated to determine their effects on the delamination, first by changing the properties of the low-k materials and then by examining more patterned layers.

As stated in the Introduction, the semiconductor industry is pursuing lower and lower dielectric constant insulator to reduce RC, which is often attained by compromising mechanical properties. It is of interest to see how the driving force for delamination changes for decreasing ILD modulus. Fig. 12 shows the effect of decreasing modulus of low-k dielectric on the energy release rate when the film structure is fixed. The peak of the energy release rates shifts higher as

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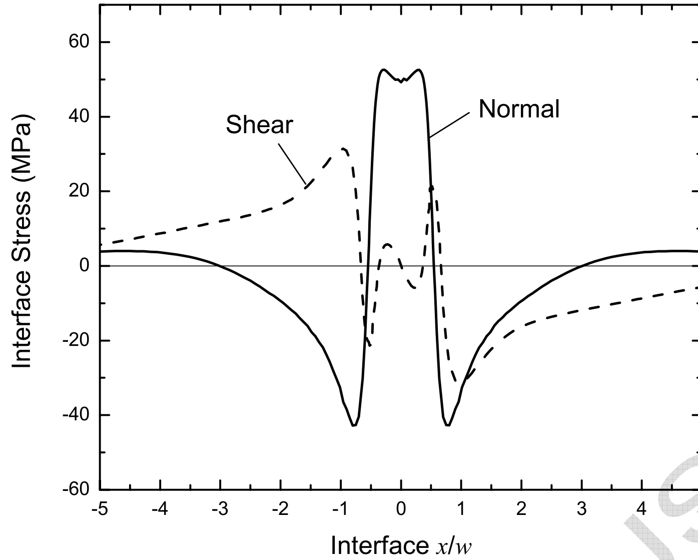

Fig. 11. Stresses on interface of low-k and cap

the modulus decreases. The maximum values occur at $2a/h = 0.88$ when the crack is close to the copper edge. It is noted that w/h is fixed at 1 in Fig. 12. If the gap spacing w changes, the peak will occur at a different crack length, such as shown in Fig. 7.

It is noted that the biaxial stress in a *blanket* film directly on a substrate is given by $\sigma = \tilde{E}\Delta\alpha\Delta T$, where $\tilde{E} = E/(1-\nu)$ is the biaxial modulus, $\Delta\alpha$ is the CTE mismatch between the film and the substrate, and ΔT is the temperature change. Therefore, in the calculations for Fig. 12, when all the material properties are kept constant as in Table 1 except the modulus of low-k material, one ends up with decreasing biaxial stress with lower modulus. The corresponding biaxial stress is listed in Fig. 12. In another set of calculations, the biaxial stress is kept constant at 43 MPa by increasing CTE simultaneously with decreasing modulus. The results obtained are plotted in Fig. 13. By comparing Fig. 13 with 12, it is obvious that increasing CTE, or equivalently, increasing the film stress of the low-k dielectric, raises the peak of the energy release rate.

In addition to the material properties of the low-k the other important aspect to consider is the increasing number of BEOL levels. Modern CMOS microprocessors, as shown in Fig. 1, have many levels of metal wiring. It is expected that the energy release rate will increase if the underlayers are stacked in such a way that causes more deformation to the overlayer. To examine this effect more underlayers are added to the structure in Fig. 5. Two cases are illustrated in Fig. 14. In one case, a blanket level is inserted below the patterned one (see Fig. 14 (a)). The additional level includes a blanket low-k film of thickness $h_1 + h$ and a cap of the same thickness h_c as the level above. In the other case

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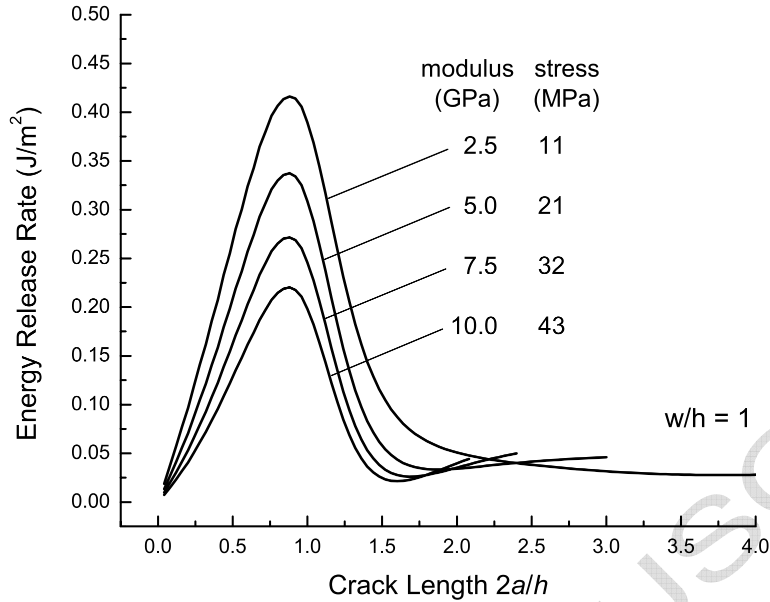

Fig. 12. Effect of reducing low-k modulus

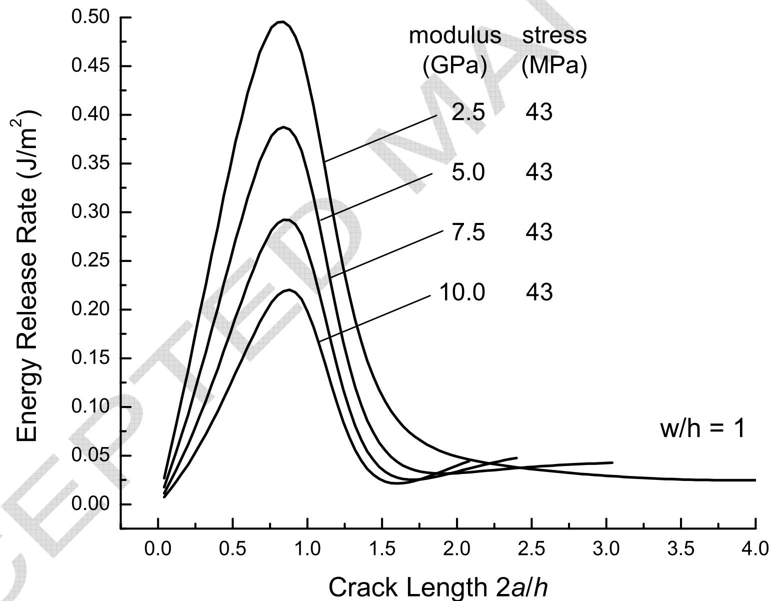

Fig. 13. Effects of reducing modulus and increasing CTE

two identical patterned levels are stacked (see Fig. 14 (b)). Another mesh similar to that for one patterned layer has been developed for both cases. Fig 14 (a) can be recovered from Fig. 14 (b) by replacing copper in the bottom level of Fig. 14 (b) with low-k material. In both cases the delamination is assumed to be between the top dielectric film and the cap. The mesh refinement follows the same schemes as in Fig. 6.

Figure 15 shows the energy release rate of three different cases of patterned films as illustrated in Fig. 5, and Fig. 14 (a) and (b). Compared to one pat-

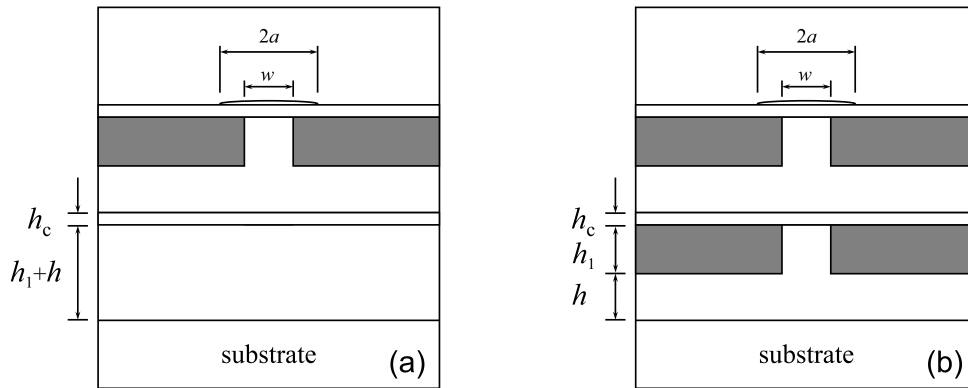

Fig. 14. Structures with more underlayers of (a) additional blanket low-k and cap film (b) more patterned low-k and cap layer

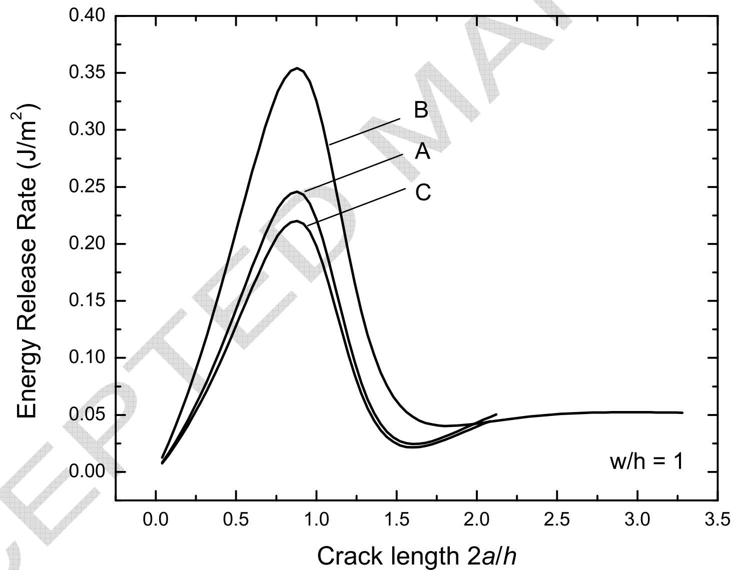

Fig. 15. Effect of more underlayers on energy release rate. Curves A and B are for geometry in Fig. 14 (a) and (b) respectively. Curve C is for geometry in Fig. 5

terned level (curve C) the energy release rate is larger in both cases of two levels of underlayers (curves A and B). It is noted that adding a patterned level increase the energy release rate more than adding a blanket one. This is because the copper plates in the patterned layer generate more stress and bending deformation in the top layer. Consequently, for the structure of two patterned underlayers, the crack closure occurs at a larger crack length.

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7 Conclusions

For a stack of blanket films, there is no driving force at all for delamination, because there is no interfacial stress and no energy is released as the interfacial defect size changes. However, when there exists a patterned underlayer, the thermal mismatch between the materials generates an interfacial stress and driving force for delamination. The driving force for delamination strongly depends on the pattern underneath.

In our model of patterned films, the cap and the top layer are pulled down by the copper plates separated by a dielectric gap. The deformation has been confirmed by AFM measurements. It is noted that the energy release rate is highly localized. It maximizes when the delamination from the center of the gap approaches the copper pad, but drops quickly as the delamination runs into the pad. The peak of the energy release rate depends on the gap spacing between the copper plates. The mode mixity varies significantly as the delamination propagates. It is predominantly under tension when the delamination is at the gap center, but becomes shear dominated as the delamination grows. On the interface of the top low-k dielectric and the cap, the shear stress changes sign and the normal stress becomes compressive as the distance to the gap center increases, indicating that the interfacial crack will arrest on the copper plate. The effects of lower modulus, higher CTE and larger film stress of low-k materials are found to increase the energy release rate. Multiple levels of patterned films also raise the energy release rate.

In all the results from our calculations, the energy release rate is less than 1 J/m^2. This is a small driving force for delamination compared to the adhesions of BEOL materials which are typically a few J/m^2. Nevertheless, if an interface is contaminated chemically during any unit process, delamination can occur during BEOL fabrication. It is noted that the delamination considered in this paper grows from the gap to the copper plate. The other direction of delamination propagation can be out of the paper plane, resulting in an interfacial tunneling crack. Since the interfacial stress due to the pattern is highly localized, the driving force for the tunneling crack is lower than the channeling crack that has been discussed in the Introduction. It is concluded that the residual stress in BEOL structures is not the dominant driving force for delamination in the test of thermal cycles of packaged chips. Instead, it comes from the stress concentration induced by packaging at the corners and edges of chips.

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