Alternatives to low-*k* nanoporous materials: dielectric air-gap integration

EXECUTIVE OVERVIEW Long considered theoretically possible, air gaps formed within multilevel on-chip interconnect structures are now under serious consideration as a means to lower the *k* value of intermetal dielectrics (IMD) for future manufacturing nodes. In fact, several integrated process flows can create air gaps, using established unit processes for deposition and etch. For example, a sacrificial material may be removed though a permeable dielectric cap, or nonconformal CVD can automatically form air gaps in properly spaced lines. Preliminary analyses of these techniques indicate that air-gap structures can be formed with acceptable yield, structural integrity, and reliability.

The continuous push for faster devices has directed interconnect technology toward the integration of porous low-*k* materials to cope with the increasing interline capacitances. The integration of porous low-*k* materials into copper dual-damascene structures is accompanied by a tremendous number of challenges [1], delaying introduction of these dielectrics, according to the *International Technology Roadmap for Semiconductors* (*ITRS*) predictions. At the end of the *Roadmap*, air gaps appear as the ultimate "porous" intermetal dielectric (IMD), since the *k* value of air is close to 1. Air gaps could be viable alternatives to fragile porous low-*k* dielectrics, with the possibility of creating lower interline capacitances provided that the structural integrity of multilayer interconnects and ultimate device lifetimes would not be compromised too much.

Air-gap integration approaches

Different air-gap integration approaches are known to fabricate multilevel interconnects. All approaches can be classified in the following categories: 1) partial or complete material removal in between metal lines followed by nonconformal CVD deposition [2, 3], and 2) damascene integration of metal lines in a sacrificial material, which can be selectively removed through a dielectric cap [4, 5].

The first class of air-gap integration makes use of the nonconformal deposition behavior of several CVD processes, where the tops of structural gaps tend to "pinch-off" such that cross-sections look like "key holes." In traditional subtractive-aluminum metallization process flows, IMD air gaps are undesirable because their uncontrolled formation can lead to metal void formation or even electrical shorts during the next metal deposition [6]. However, due to the continuous downscaling of interconnects and the accompanied increase in the interline capacitance, air gaps formed by nonconformal CVD become attractive even in aluminum metallization [7, 8].

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Figure 1 shows this specific air-gap integration approach. The basic principle consists of dielectric material removal after damascene Cu formation, followed by nonconformal CVD deposition and a final planarization step. The major variation in this approach is whether the initial IMD is removed completely or partially. By complete removal of the IMD, followed by PECVD deposition of SiCN and SiO_2, air gaps are automatically formed in the narrow intermetal spacings (**Fig. 1e**), while the wider spacings are completely filled (not shown).

The second air-gap integration approach involves the removal of a sacrificial IMD layer through a permeable cap. As shown in **Fig. 2**, this integration route might require a protective cap for the exposed copper lines. Removal of dense dielectrics from the complete stack by using selective caps enables removal of all sacrificial IMD layers

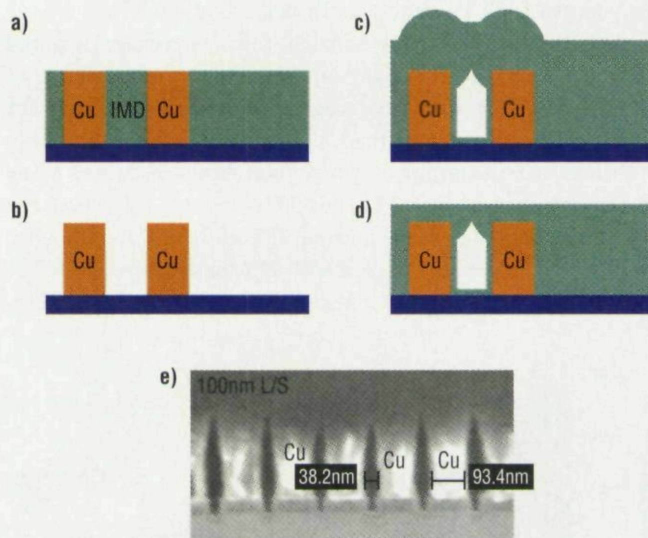

Figure 1. a–d) Schematic representation of the formation of air gaps by means of nonconformal CVD, and **e)** SEM cross-section showing fabricated structures.

at multiple metal levels after full completion of the stack, though the sacrificial IMD removal may be done after completion of each metal level. In the latter case, since IMD removal can occur after metal CMP [4], the use of a self-aligned barrier is not required when a permeable hard mask is used on top of the IMD (**Fig. 2e**).

Different approaches exist to remove the sacrificial layer through the cap. In one, a thermal degradable polymer is used [4, 9], which can be decomposed by heat (optionally in combination with UV) through a porous dielectric cap (Fig. 2e). However, the sacrificial layer might

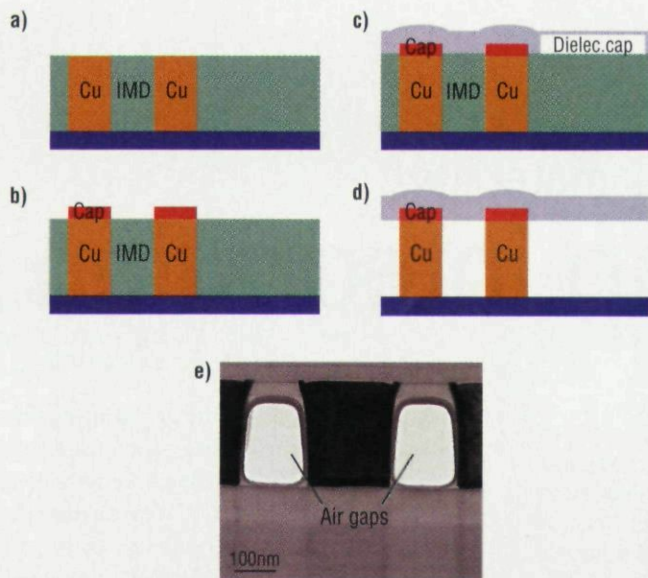

Figure 2. a–d) Schematic representation of the formation of air gaps by selective IMD removal through a dielectric cap, and **e)** SEM cross-section showing fabricated structures.

also be removed by selective (wet or dry) etching through the cap.

System-level considerations

The interconnect performance can be benchmarked using the RC-product of different interconnect architectures. For low-power applications, the interconnect capacitance (*C*) is more important than interconnect resistance (*R*) from a system perspective [10], so air gaps are especially interesting for these kinds of systems.

A commercial interconnect analysis software package (Raphael) was used to simulate the k_{eff} for air-gap architectures consisting of two metal levels at 45nm technology node dimensions (**Fig. 3**). For structure D using nonconformal CVD, the width of the air-gap cavity is assumed to be 30nm and to extend 20nm above the Cu lines, while the air-gap cavity at IMD2 extends 50nm into the ILD1 level. For structure F using sacrificial material, 75% of the IMD1 and IMD2 thickness is composed of air gaps, with 90% for structure H.

The k_{eff} at M1 is somewhat higher than at M2 for all structures

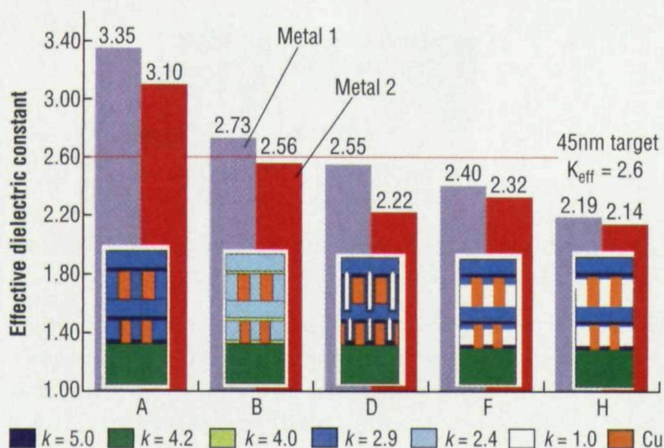

Figure 3. Simulated effective dielectric constants (k_{eff}) for various two-metal-level interconnect architectures at the 45nm node for **A)** dense low-*k*, **B)** porous low-*k*, **D)** CVD pinch-off air gaps, and **F-H)** sacrificial removal air gaps. At M1, L/S = 65/65nm, IMD = 140nm thick, via diameter = 70nm, 105nm deep. For M2, L/S = 80/70nm and ILD = 170nm thick.

in Fig. 3 due to the fringing capacitances through the pre-metal dielectric and bottom SiC liner. Even structure B, using a porous low-*k* material with a bulk 2.4 *k* and a SiC(N)-cap with 4.0 *k* is barely able to meet the requirements. The only architectures where k_{eff} is below 2.6 for both M1 and M2 are achieved using air gaps.

The nonconformal CVD approach gets most of its gain through reduction of the fringing capacitance due to the gap extension above and below the IMD level. A further decrease might be possible by complete material removal combined with extreme nonconformal CVD [11]. The sacrificial approaches have the biggest gains, since they benefit from the removal of dielectric from the complete IMD width.

Mechanical integrity

One of the biggest concerns with respect to the introduction of air gaps in interconnects is the mechanical integrity of the entire stack. Due to weaker mechanical properties of the dielectric materials, packaging process steps such as wire bonding and molding might induce cracks inside the IC stack and therefore create electrical failures in the short or longer term. Good mechanical properties of the stack are therefore essential for chip survival during packaging [12].

With sacrificial-material air gaps, the mechanical strength of the stack is solely determined by the metal and other cap/barrier dielectrics. Exact placement of the air gaps in specific locations on each metal level is therefore of great importance and will determine the mechanical integrity of air-gap interconnects. The mechanical integrity can also be enhanced by the use of an additional mask to prevent dielectric removal in noncritical areas of medium or large line spacing.

The mechanical integrity is less problematic for the nonconformal CVD approaches compared to the sacrificial material approaches, since the CVD dielectric contributes to the mechanical strength of the stack in wide spaces. Regardless of the approach, the mechanical strength of air-gap layers depends on the placement of metal structures. For air-gap integration, a design trade-off is needed between minimal routing-area (functionality-aware design) and sufficient metal density to ensure good mechanical strength of the entire stack (air-gap-driven design).

Some applications do not require many air-gap metal layers; the incorporation of one air-gap level might be sufficient for the required performance boost and/or power reduction. From low-*k* packaging experiments, it is well known that most of the failures occur in the top levels. Therefore, one could opt for only a few air-gap layers at the lowest metal levels.

Reliability challenges

In addition to challenges related to mechanical integrity, concerns exist that air gaps might give rise to long-term reliability problems. Device lifetimes could theoretically be reduced due to electromigration failures and degraded barriers.

Via reliability. Unlanded vias are major concerns in air-gap integration, since the potential misalignment of line and via levels could allow via etch to open a pathway to an air gap. Wet chemicals could then remain trapped inside the air gap and cause long-term barrier corrosion. Moreover, a thin metallic barrier can never close this undesired pathway, resulting in a barrier discontinuity.

For most air-gap architectures, the unlanded via issue can be overcome by using more space for the via landing. This space can either be a copper landing pad or a dense dielectric that has not been

continued on page 58

Dielectric air-gap integration continued from page 56

removed prior to air-gap formation. However, the drawback of this solution is that the extra space takes up routing area.

For the nonconformal CVD approaches, the deposited dielectric on the sidewall (before pinch-off) provides some margin for via landing. This may not be a scalable option, however, since the thickness of sidewall dielectric decreases as the dielectric spacing is scaled down. For sacrificial material approaches, fewer issues are expected with unlanded vias since the sacrificial material is not yet removed at the stage of via etch in most cases.

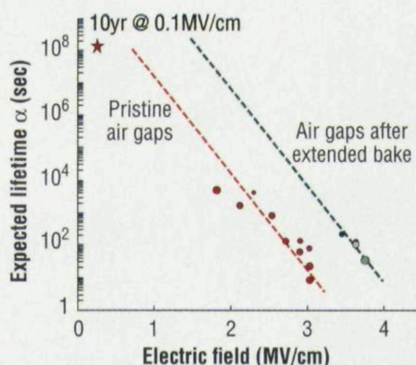

Figure 4. Failure times versus electric field for a 150nm air-gap space (for pristine samples and for samples that received an extended bake prior to TDDB measurements).

Electromigration. Hau-Riege et al. [13] stated that copper embedded in low elastic modulus materials would result in shorter electromigration (EM) lifetimes due to the lower "back stress" of the surrounding material. Since air gaps have little or no material to provide support, the entire back stress has to come from the metallic barrier. Consequently, EM lifetimes would theoretically decrease with thinning of the metallic barrier, leading to another potential scalability issue.

From work on air gaps formed by nonconformal CVD in between aluminum lines [14], it is known that the EM lifetimes of air-gap structures (especially for the case of narrow and high aspect-ratio lines) are significantly higher than for solid gap-filled interconnects. Failure analysis and simulation results indicated that the compliant sidewall of the air gap is able to deform and relieve the stress during metal depletion. Copper/air-gap interconnect structures formed by nonconformal CVD show no significant difference in lifetimes as compared to dense references [2]; no new failure modes, such as metal extrusion between the lines, were observed.

For sacrificial-material air gaps, the situation is expected to be the same or worse, since no dielectric exists to support the metallic barrier at the sidewalls. However, first preliminary EM experiments using packaged samples on 200nm wide lines surrounded by 250nm wide air gaps gave promising lifetimes with a MTTF of 228 years and a 0.01% failure after 6.5 years [4]. SEM inspections after EM tests have revealed two types of damage: void formation near the cathode side, and copper extrusions in the second part of the line. Nevertheless, the EM lifetime does not seem to be affected too much by the fact that the metal lines are embedded in a mechanically weak material (or no material at all).

Interline leakage and air-gap breakdown. For nonconformal CVD air gaps, leakage current and shorts were found not to be problematic by Noguchi et al. [15]. They demonstrated that the time-dependent breakdown (TDDB) of nonconformal CVD air gaps considerably outperformed that of interconnect using conventional FSG dielectric. The leakage current of the air gaps was found to be lower than that of FSG at high voltage, probably because the trap-assisted conduction mechanism is hampered. Short cuts between adjacent lines occur less frequently since metallic residues in between the lines will be removed during the gap etch.

However, it should be mentioned that leakage, breakdown strength, and especially TDDB are extremely sensitive to moisture inside the gaps. **Figure 4** shows that TDDB lifetimes can be considerably improved if moisture is removed from the inside of the integrated structures by a bake step. Therefore, moisture should be kept out of interconnect structures containing either low *k* or air gaps.

Conclusion

Two different air-gap integration approaches were investigated in detail. The first class uses sacrificial materials, which are selectively removed through a capping layer either by wet- or dry-etching or by thermal decomposition. The second class uses the nonconformal deposition of different CVD layers, which creates air gaps for narrow spaced lines. All approaches show significant IC performance increases through capacitance reduction. Interconnects containing air gaps do not show more reliability challenges than interconnects with porous low-*k* dielectrics. Therefore, air-gap technology is a viable option for the 32nm node and beyond. ■

Acknowledgments

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References

1. R.J.O.M. Hoofman, G.J.A.M. Verheijden, J. Michelon, F. Iacopi, Y. Travaly, M.R. Baklanov, et al., *Microelectron. Eng.* 80, pp. 337–344, 2005.
2. V. Arnal, J. Torres, P. Gayet, R. Gonella, P. Spinelli, M. Guillermet, et al., *Proc. IITC*, pp. 298–300, 2001.
3. J.P. Gueneau de Mussy, C. Bruynsereade, Z. Tokei, G.P. Beyer, K. Maex, *Proc. IITC*, pp. 150–152, 2005.
4. R. Daamen, G.J.A.M. Verheijden, P.H.L. Bancken, T. Vandeweyer, J. Michelon, V. Nguyen Hoang, et al., *Proc. IITC*, pp. 240–242, 2005.
5. L.G. Gosset, A. Farcy, J. de Pontcharra, Ph. Lyan, R. Daamen, G.J.A.M. Verheijden, et al., *Microelectronic Engineering* 82, pp. 321–332, 2005.
6. D.R. Cote, S.V. Nguyen, W.J. Cote, S.L. Pennington, A.K. Stamper, D.V. Podlesnik, *IBM J. Res. Develop.* 39, pp. 437–464, 1995.
7. B.P. Shieh, L.C. Bassman, D.-K. Kim, K.C. Saraswat, M.D. Deal, J.P. McVittie, et al., *Proc. IITC*, pp. 125–127, 1998.
8. T. Ueda, E. Tamaoka, K. Yamashita, N. Aoi, S. Mayumi, *Proc. VLSI Symp.*, pp. 46–47, 1998.
9. P.A. Kohl, D.M. Bhusari, M. Wedlake, C. Case, F.P. Klemens, J. Miner, et al., *IEEE Electron Dev. Lett.* 21, pp. 557–559, 2000.
10. V.H. Nguyen, P. Christie, A. Heringa, A. Kumar, R. Ng, *Proc. IITC*, pp. 191–193, 2005.
11. A. Stich, Z. Gabric, W. Pamler, *Microelectron. Eng.* 82, pp. 362–367, 2005.
12. L.L. Mercado, C. Goldberg, S.M. Kuo, T.Y. Lee, S.K. Pozder, *IEEE Trans. Dev. Mater. Reliab.* 3, pp. 111–118, 2003.
13. C.S. Hau-Riege, S.P. Hau-Riege, A.P. Marathe, *J. Appl. Phys.* 96, pp. 5792–5796, 2004.
14 B.P. Shieh, M.D. Deal, K.C. Saraswat, R. Choudhury, C-W. Park, V. Sukharev, *Proc. IITC*, pp. 203–205, 2002.
15. J. Noguchi, K. Sato, N. Konishi, S. Uno, T. Oshima, K. Ishikawa, *IEEE Trans. Electron Dev.* 52, pp. 352–359, 2005.

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